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Development and Testing of an Ultra Low Power System-On-Chip (SOC) Platform for Marine Mammal Tags and Passive Acoustic Signal Processing

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LONG-TERM GOALS

The long term goal of this project is to develop and build an ultra-low power system-on-chip (SoC) that will increase the useful lifetime of animal tags for monitoring marine mammals to weeks or months and to integrate that chip into a new monitoring tag, called Nano-power Electronics MOdule (NEMO). The NEMO tag has the specific application goal of determining the response of deep diving whales to human generated acoustic events, although the tag and SoC will be programmable to support numerous other monitoring applications. The final goal is to provide fundamental research into the optimal tag partitioning between custom and off-the-shelf components, novel analog/digital co-design for acoustic event detection, and ultra-low power on-chip power and event management control to extend the lifetime of tags like NEMO as much as possible.

OBJECTIVES

- Provide a low power processing platform for marine mammal tags.
- Identify methods for optimal low power partitioning of digital and analog computation
- Develop power saving schemes for on chip computation to save energy related to data storage in an off chip non volatile memory (NVM)

- Demonstrate an integrated SoC for marine mammal tags
- Integrate the SoC into a prototype tag (called NEMO)

APPROACH

Our approach to lowering marine mammal tag power consumption is to develop a programmable ultra low power (ULP) SoC to enable intelligent data collection, event detection, feature extraction, and power management in marine mammal monitoring tags. This SoC will reduce processor power by implementing a custom ULP processor using sub-threshold operation, and it will reduce NVM power and capacity limitations by allowing for programmable event detection and information extraction on chip to cut the volume of data going to the NVM by many orders of magnitude.

The proposed SoC will include on-chip digital processing for dive profiling, local memory, hardware acceleration for data processing, and I/O interfaces to external NVM and peripheral components. In a modification to the original system architecture, the low power analog interface to external sensors and analog-to-digital conversion (ADC) is moved to a separate chip with a low power chip-to-chip digital interface. Figure 1 shows a block diagram of the SoC based system. The digital portion of the chip includes a general purpose microcontroller for fully programmable processing and control. A special purpose digital power management (DPM) block oversees mode changes and manages energy consumption in the various blocks. One primary mechanism for this is the use of power gating header switches to cut off the voltage supply from any unused blocks, reducing the active and leakage energy consumption of those blocks by orders of magnitude. On-chip SRAM, managed by a direct memory access (DMA) controller, provides instructions for the microprocessor and DPM and serves as local storage for buffering acquired data prior to sending it out to off chip non volatile memory (NVM) storage.

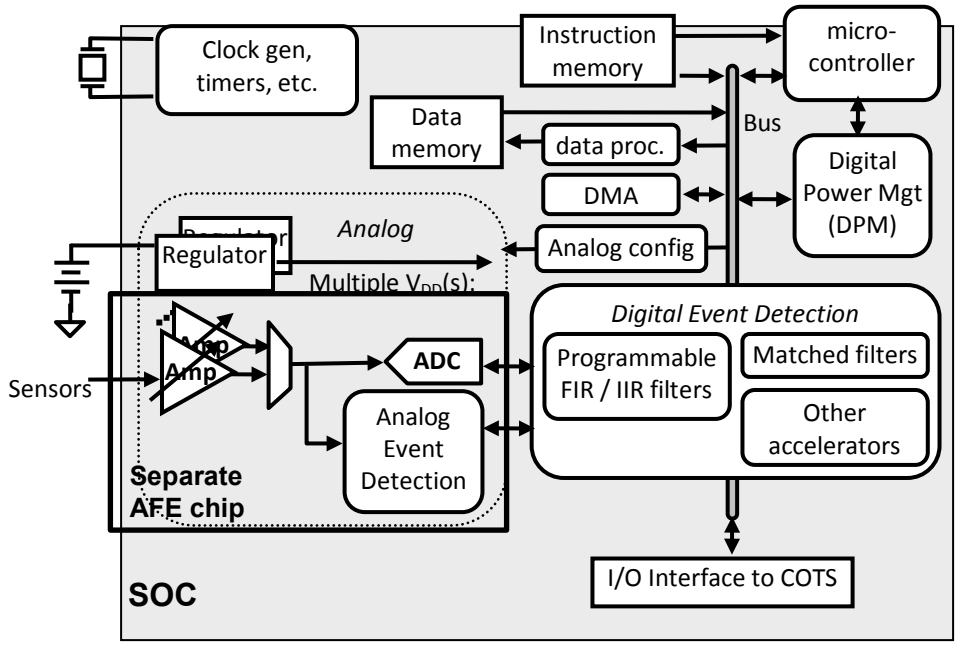


Figure 1. Block diagram of the proposed SoC for marine mammal tags.

Now that the NEMO SOC chip and the sensor AFE chip are developed and tested, we envision integrating them on a small circuit board with an integrated hydrophone and pressure sensor, along with other inertial sensors that can be switched off. To minimize power draw, we will continually record dive parameters at a user-defined sample interval, such as every 1 second. These values will be stored to the onboard memory on the chip. When the buffer is full, these will be transferred to flash memory on the board (either microSD card or IC flash memory). We will also implement the histogram technique to reduce the amount of data that needs to be stored, and thus power requirements. The hydrophone will be operated continuously and the chip will be used to detect echolocation clicks and low-frequency sonar-like signals (narrow band signals). We will implement a full range of functionality, from storing raw hydrophone signals, to storing metrics of event detections, such as timing of echolocation clicks and peak amplitudes. For narrow band FM signals we would store peak frequency, amplitude, and duration along with a timestamp. The ultimate goal is to produce a tag that is capable of being programmed in a number of different ways, ranging from continuous recordings similar in capabilities to existing acoustic recording tags (but with greatly reduced power consumption), to user-defined detection and data reduction on the tag.

WORK COMPLETED

Our proposed goals for the third full year of this project were to tape out and measure a revised low power analog front end for the acoustic and depth sensors, to characterize the first hardware for the platform SOC, and to plan for integration of these chips into the full NEMO system.

We have accomplished these goals and now have measured results from both chips. We are ready to move forward with integration of the chips into a system.

Our major accomplishments this year are as follows:

- Measured the complete NEMO SOC, made fixes to bugs, and taped out a new SoC chip (meets proposed goal)
- Developed revised design for analog front end for hydrophone and depth sensor (meets proposed goal)
- Taped out and tested revised analog front end chip (meets proposed goal)
- Implemented and tested SPI for communication off chip (meets proposed goal)
- Successfully tested full SOC (meets proposed goal)

In the rest of this section, we describe the different areas of the project in more detail.

RESULTS

The AFE chip demonstrated last year functioned correctly, but its noise performance was not as good as we hoped to achieve for sensing hydrophone data. To correct this and to improve the interface between the AFE chip and the SoC, we re-designed the AFE chip and re-fabricated it this year.

Additionally, the SoC chip experienced a memory problem that we described last year (resulting from a large process skew and insufficient design margin in a pulse generator). We redesigned the memory,

fixed several other problems with power gating switches in the SoC, and refabricated the SoC this year. The SoC and AFE chips were designed to interface through a low power SPI bus.

NEMO System Level Integration Plan

Figure 2 shows the system-level block diagram that includes the SoC and the AFE chip, which was broken off onto a separate chip for implementation and testing convenience. The AFE chip includes the analog front end interfaces to both the depth sensor (piezo sensor) and the hydrophone. The outputs of these AFEs are multiplexed to an ADC, digitized, and then communicated off chip via either a SPI interface or a serial debug interface. The SoC acts as a system level controller to manage the operation of the node. The SoC initiates transfers from the AFE to acquire hydrophone and piezoelectric sensor data.

After the data has been received, the SoC can digitally process the data using on-chip hardware accelerators and perform feature extraction to determine if a significant event has occurred such as a dive or a sonar event. Specifically, the dive profile block can store up to three histograms of data including the duration of dives, the maximum depth of each dive taken, and the time at depth. This block has a programmable dive threshold to determine what depth is considered a "dive event". It can also be programmed to have up to 20 histogram bins and set the number of dives taken before an interrupt event occurs to wake up the MCU.

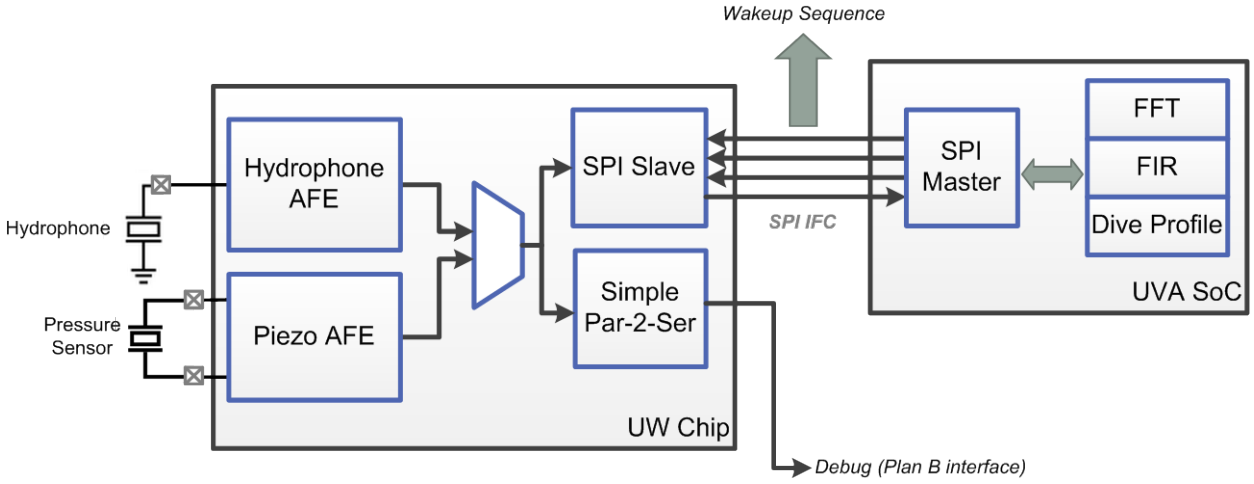


Figure 2: System integration block diagram showing chip-to-chip communication scheme.

AFE Digital Interface

To interface to the SoC, the AFE chip needed a digital interface, and we selected SPI as the lowest energy option. Figure 3 shows a block diagram of the digital portion of the AFE chip. The AFE side of the system includes a SPI slave module that allows the user to configure the AFE and retrieve hydrophone or piezoelectric sensor data. There is a backup serial interface that serializes any incoming data and pushes it out at the current system clock rate. Since this was a test chip, we included both a "test" and "deployment" mode. There are internal muxes to determine whether the inputs to the system come from pads (test mode) or from the SPI module (deployment mode). The muxes internal to this block are controlled by the memory–mapped registers that can be written to via the SPI slave module. There is also additional configuration for the amplifier gain, power gating, and the clock rate (clock dividers). This digital interface allows the SoC to maintain sophisticated control over the functionality of the AFE including power management options, providing for system level efficiency.

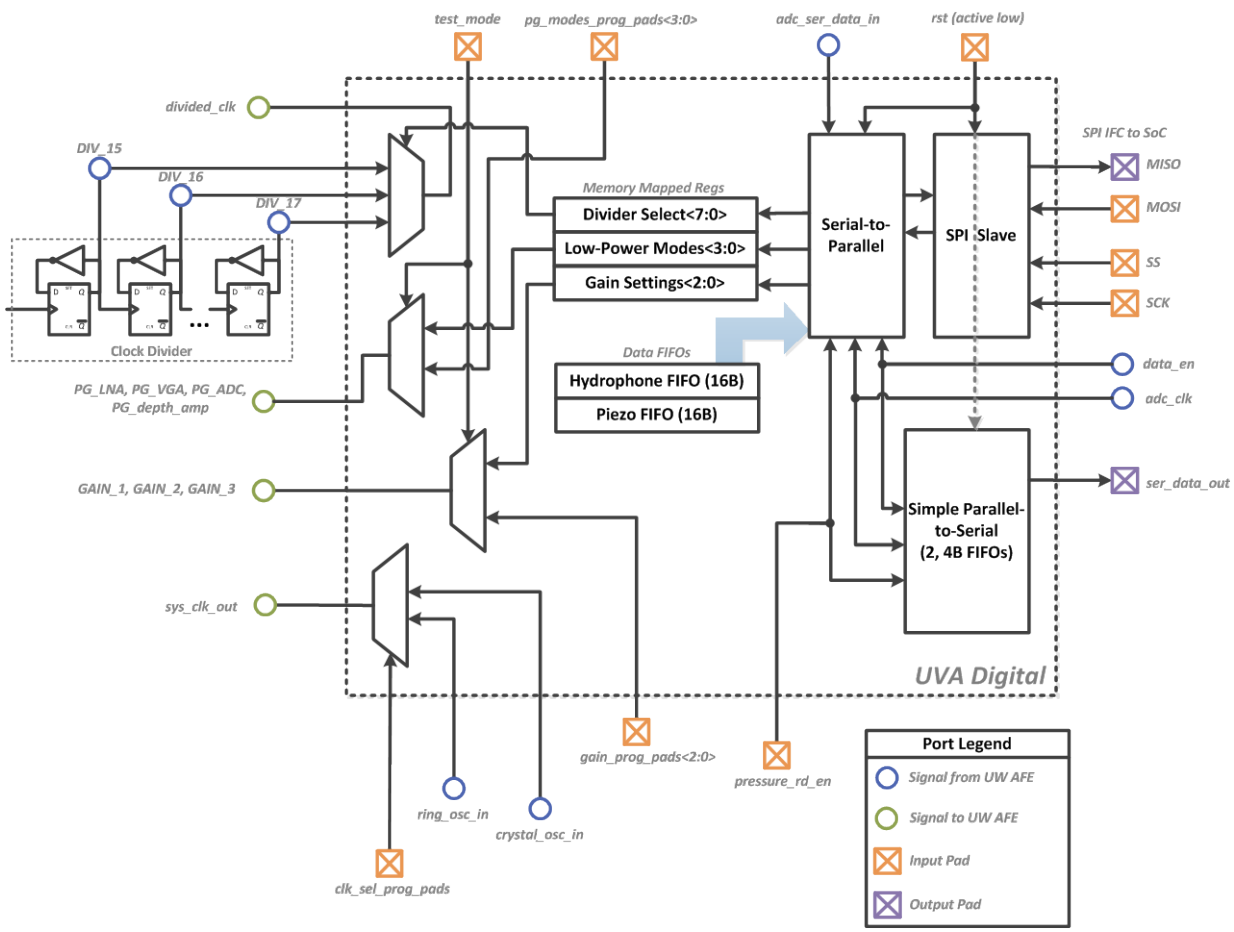


Figure 3: Detailed block diagram showing the digital interface and control integrated on the AFE chip.

Figure 4 shows a timing diagram of the system taking ADC data and serializing it using the simplified serial interface is shown below. This shows the ADC data being parallelized, an enable signal going high to indicate the start of a new transfer, another bit being pulsed high to indicate the type of data being transferred (piezoelectric or hydrophone), and then the data is streamed from the ser_data_out port.

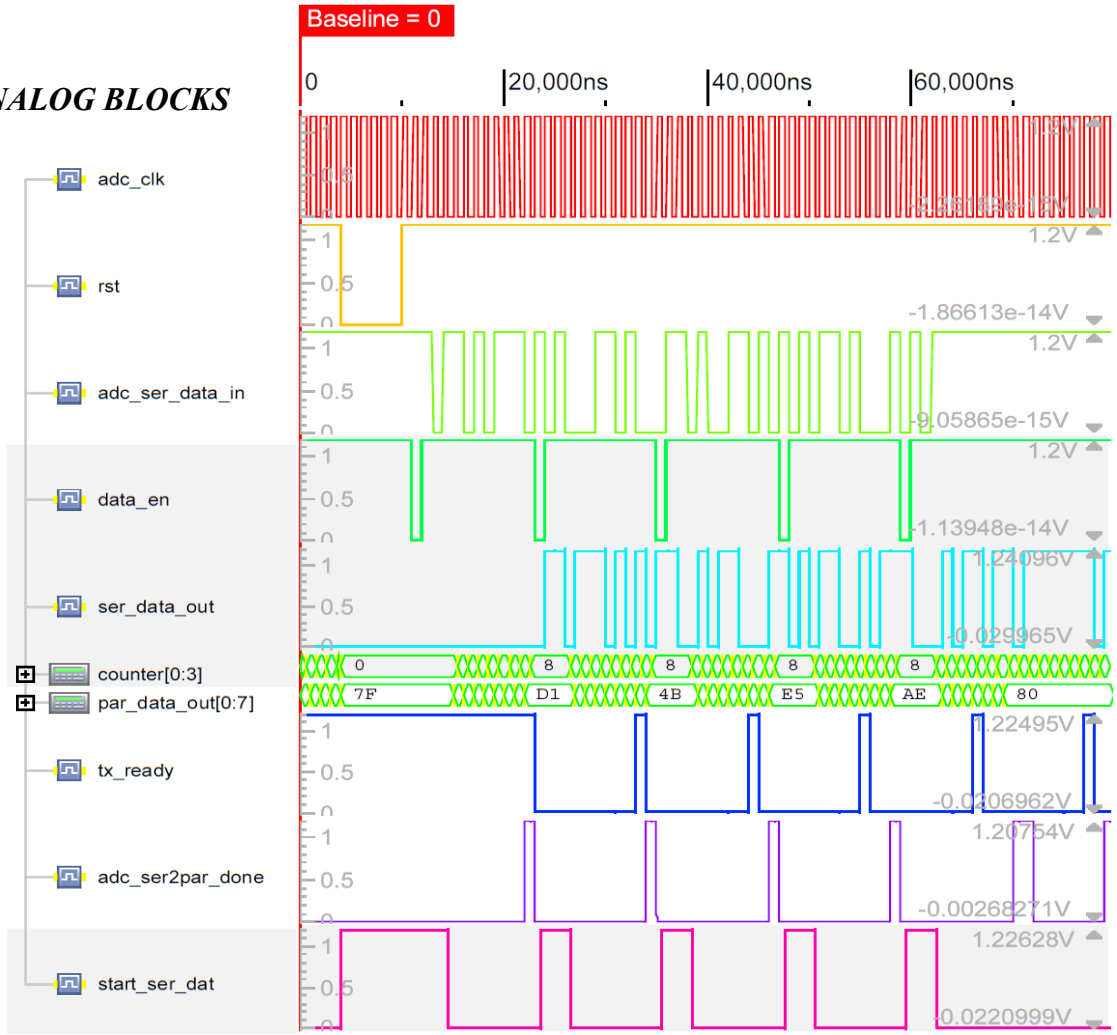


Figure 4: Timing diagram showing system integration (simulation) between the AFE chip and the SoC.

AFE Chip Block Diagram and Schematic: The revised analog front-end (AFE) for the NEMO project consists of a hydrophone AFE, depth sensor AFE, ADC, and Slave SPI as shown in Figure 5. This chip incorporates redesigned versions of the three amplifiers from the AFE chip last year, with the designs optimized to improve noise performance. It also includes additional components for better interfacing with the SoC, as described in the previous section.

The hydrophone AFE consists of a low noise amplifier (LNA), anti-aliasing filter, and variable gain amplifier (VGA). An 8-bit successive approximation register (SAR) ADC is implemented for signal digitization. The sampling frequency can be programmed by using an internal ring oscillator or external crystal oscillator. The AFE chip was fabricated on a standard 130 nm CMOS technology, and

Figure 6 shows the die photograph (left) and the test printed circuit board (PCB) design for testing each block on the AFE chip independently.

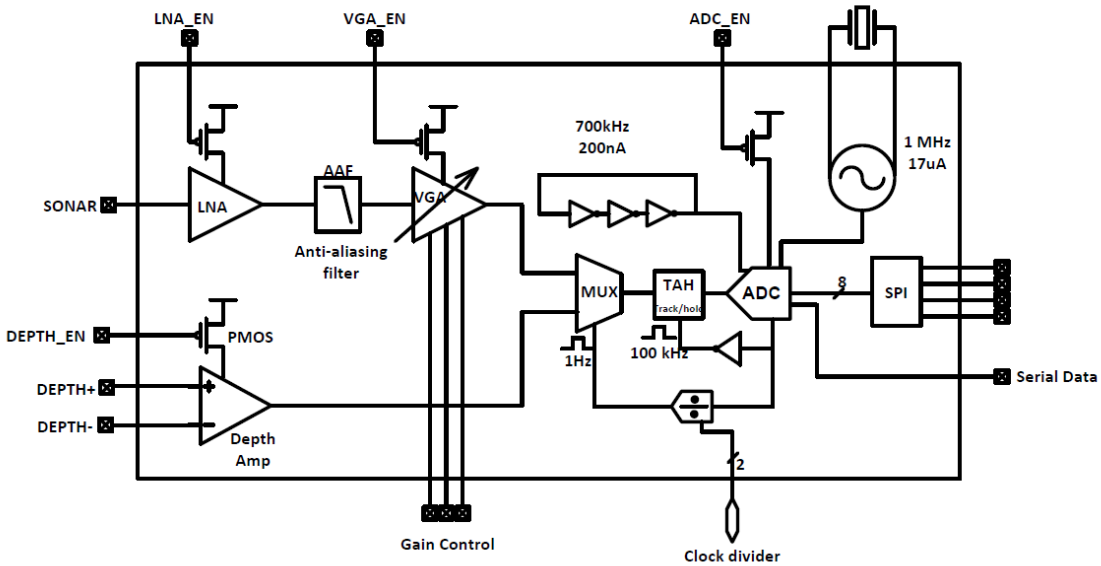


Figure 5: Analog front-end chip block diagram

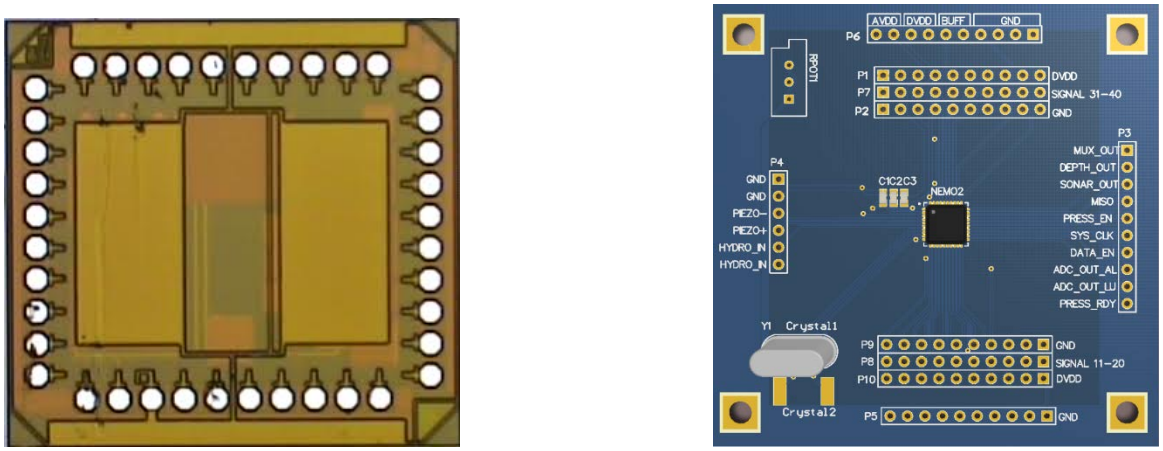


Figure 6: Die photograph and PCB design for new AFE chip.

AFE MEASUREMENT RESULTS

The following measurements were obtained using Agilent's Dynamic Signal Analyzer (DSA) 35670A and Mix Signal Oscilloscope DSO7104B. With this equipment, we measured the power noise as well as frequency response. However, this equipment is frequency limited as it is only capable of measuring from DC to 52.1 kHz.

Hydrophone AFE Noise performance

On Figure 7, we observe that the output referred noise at 10kHz for high-gain mode in the hydrophone is 18.1uV/rt(Hz), and the output referred noise at 10kHz for low-gain mode is 1.5uV/rt(Hz). The

hydrophone detection is performed by a low-noise front-end that achieves an input-referred noise of 18.1 nV/√Hz at 10 kHz. For comparison, a Texas Instruments' low-power, low-noise 1.8V Op-amp (OPA2314) achieves 13 nV/√Hz at 10 kHz. The power consumption for these two amplifiers is also comparable, 193.4 µA (this work) vs. 150 µA (TI's). One notable advantage of the analog-front-end presented in this work compared with similar systems is the relatively high gain achieved (Figure 9). The first stage consisting of an LNA contributes a static gain of 40.6 dB while the second stage contributes a variable gain of 38.2 dB achieving a maximum voltage gain of 78.8 dB. This nearly 10000x of amplification capability, combined with a low-noise front-end enables this system the ability to detect distant sonar signals. In comparison, TI's part is only 20dB. Moreover, given that the gain can be automatically configured means that the amplification can be scaled down for nearby acoustic sources.

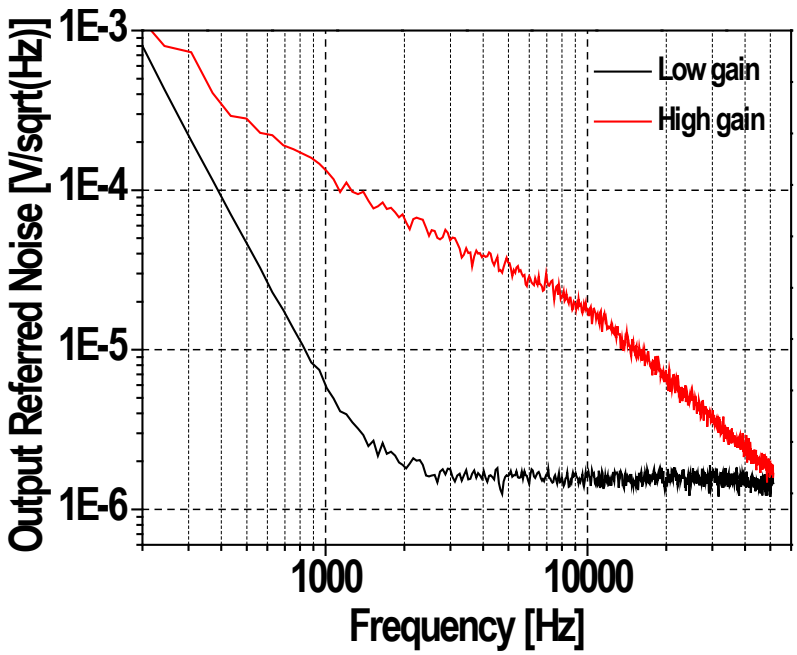


Figure 7: Hydrophone AFE noise performance

Depth sensor AFE noise performance

On Figure 8, we observe that the output referred noise at 10kHz for high-gain mode is 25.8uV/rt(Hz), and the output referred noise at 10kHz for low-gain mode is 17.4uV/rt(Hz).

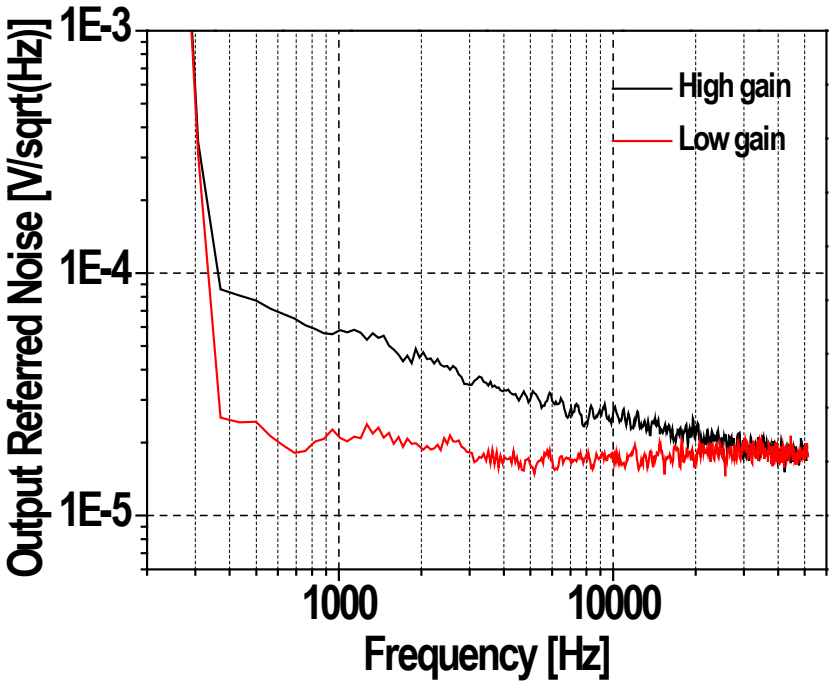


Figure 8: Depth AFE noise performance

Hydrophone AFE Gain

On Figure 9, we observe that the minimum gain (black curve) at 1kHz is 40.6 dB, and the maximum gain (red curve) at 1kHz, which is directly measured from the DSA, is 66.3 dB. We observed that the output signal in the high-gain mode is saturated even with the minimum input level of 150µV. Thus, we use a resistor voltage divider at the input to attenuate the DSA source level, and we measured the highest voltage gain (blue curve) is 78.8 dB.

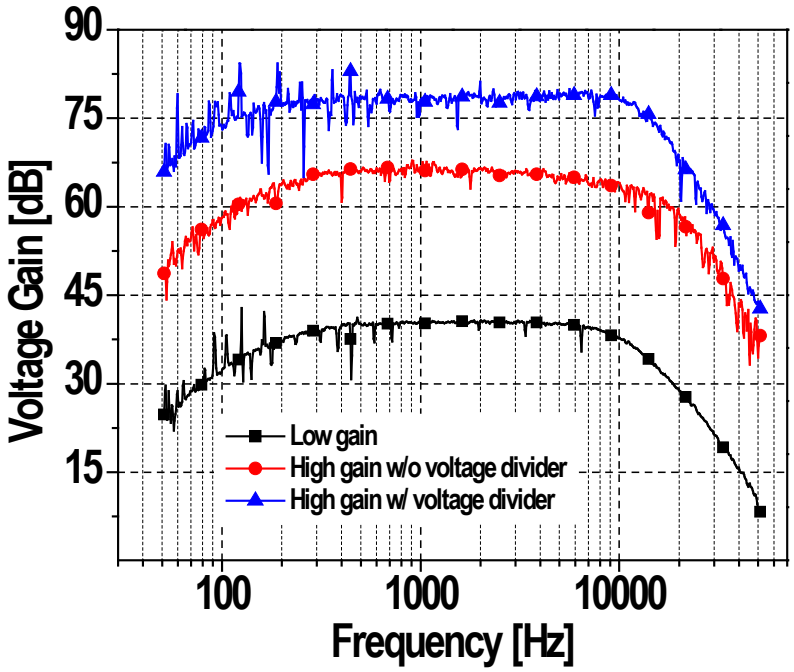


Figure 9: Frequency Response — Hydrophone AFE

Depth sensor AFE Gain

On Figure 10, we observe that the minimum gain (red curve) at 1kHz is 6.4 dB, and the maximum gain (black curve) at 1kHz which is directly measured from the DSA is 24.3 dB.

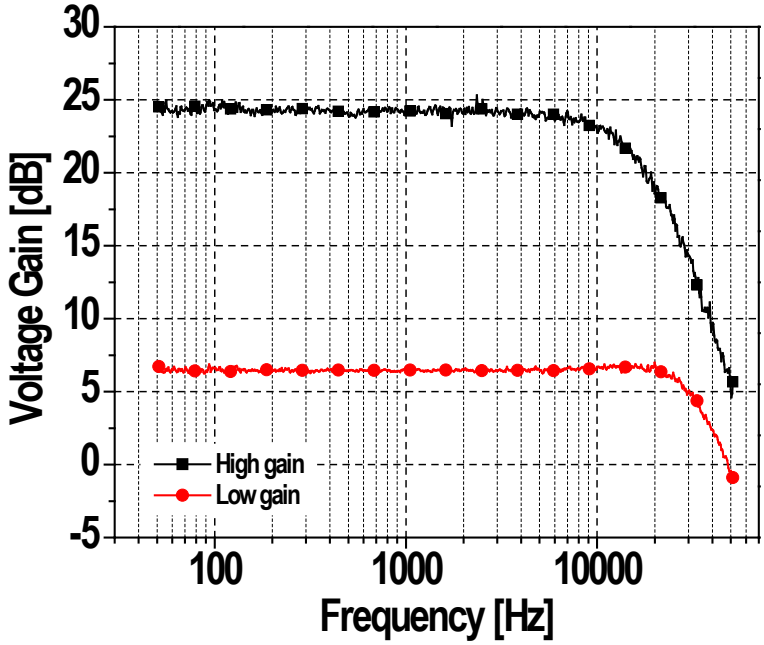


Figure 10: Frequency Response—Depth AFE

Oscillator Performance

Figure 11 shows the measured waveform of ring oscillator. The oscillator frequency is 460 kHz.

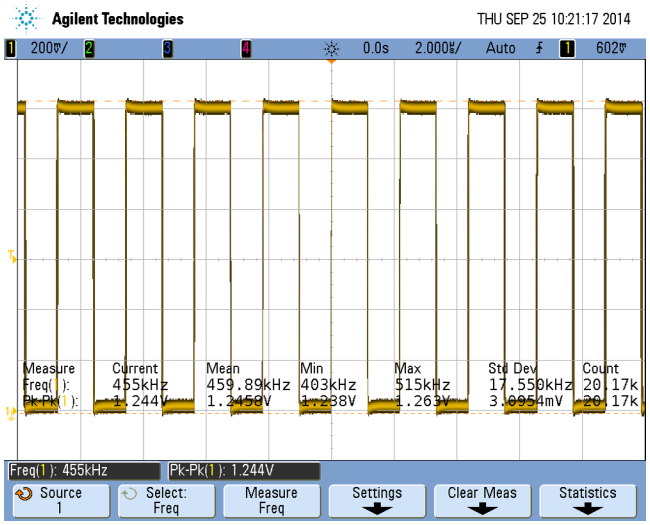


Figure 11: Ring oscillator measurement

Figure 12 shows the measured waveform of the crystal (XTAL) oscillator. The XTAL oscillator frequency is 1MHz.

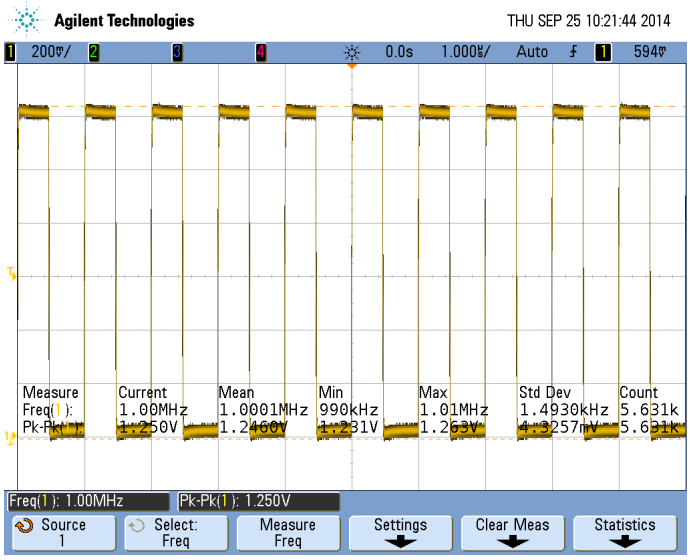


Figure 12: Crystal oscillator measurement

ADC Measurements

Figure 13 and Figure 14 shows the ADC measurement setup and results. The frequency of the signal at the input of the hydrophone AFE is 10 kHz with peak-to-peak amplitude of 1mV. At the output of the MUX, we observe peak-to-peak amplitude of 410mV. Figure 14 shows the measured serial data at the output of the ADC, confirming its correct operation.

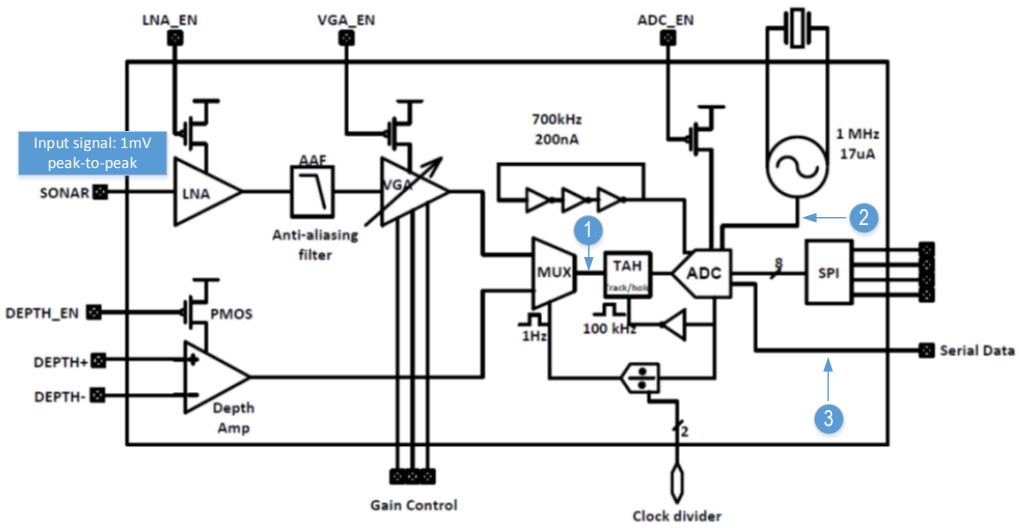


Figure 13: Setup for ADC measurement

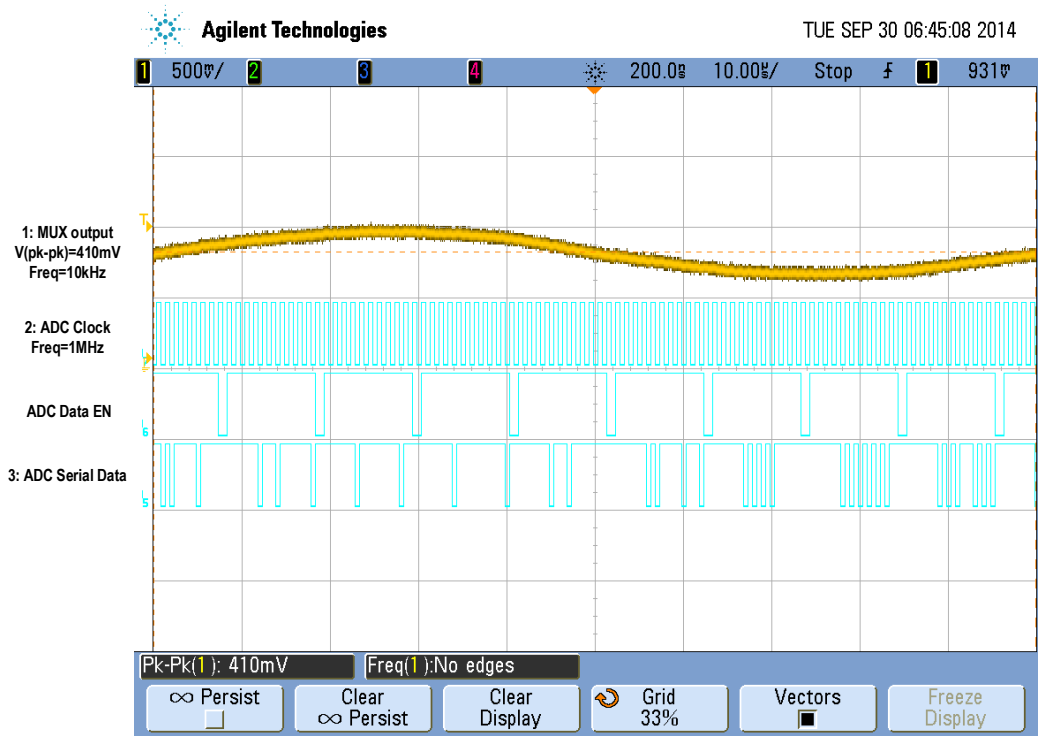


Figure 14: ADC serial data measurement

The current consumption of the AFE chip is shown below:

Block	Current Consumption (µA)
VGA	65.3
LNA	193.4
Depth Amp	71.6
ADC	0.3
Clocks	22.6
Rest of Circuit	83.3
Total	**436.5**

This report presents the measurement results for the second iteration of this AFE. Compared to the first AFE chip presented last year, this IC offers several improvements in terms of noise, power consumption and the adaptation of a digital interface and signal digitization. First, due to a low gain of only 17.8 dB of gain, 100 nV/√Hz was measured in the first chip. In comparison, for this latest work a maximum gain of 78.8 dB of gain results in 18.1 nV/√Hz. Second, the power consumption for the hydrophone amplifier presented last year was reported to be 758 µW, which was reduced to 231 µW. Also, the total AFE power consumption in this latest AFE is 524 µW compared to 1.04 mW in the first run. Third, the most notable improvement made to this AFE over the one presented last year is signal digitization and the ability to digitally configure gain, power gating (for low-power mode) and frequency scaling. In summary, we have completed the fabrication of an AFE interface chip for low power hydrophone and depth sensing. We have performed characterization measurements of all of the blocks on the chip and confirmed that they are functioning correctly and with good performance specifications. The next step is to interface the AFE chip with the SoC to build the NEMO system.

PLATFORM SYSTEM ON CHIP (SOC) DEVELOPMENT

This year we achieved system level measurements for the platform SOC that is the core of the NEMO tag. The design adhered to the vision from Figure 1. Figure 15 shows a die photograph of the SoC. For hardware development, this year we have successfully tested the system on chip (SoC) for histogram collection, dive profile processing, and (dual use) wearable physiological monitoring. The initial chip design taped out in 2013 suffered a few minor design bugs that we fixed for a follow-on tapeout this year. These bugs included the SRAM timing issue described last year and missing header switches that left two blocks (SPI and low power MCU) non-functional. These bugs are now all corrected and working in hardware.

The chip is approximately 3.5mm x 3.6mm and has over 2.2 million transistors. It has 4kB of data memory, 4kB of instruction memory, and a 2kB high speed buffer for streaming data off chip to a NVM. It has a programmable 16b MSP430 microcontroller and hardware accelerators for programmable FFT, FIR filtering, Cordic co-processing, and aggregating dive profile data.

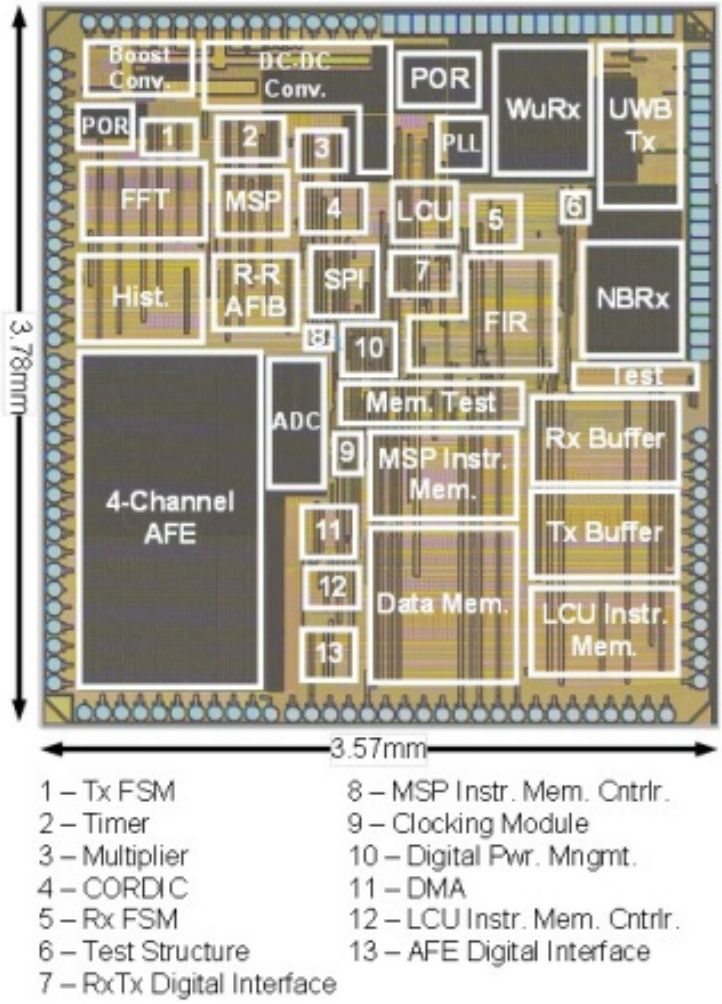


Figure 155. Annotated die photograph of the SOC for the NEMO platform, which doubles as a wearable physiological sensor.

System-level architecture

The system-level architecture for the chip contains two, independent bus structures. The first bus is controlled by either the openMSP430 or the Lightweight Controller Unit (LCU), and the second bus is driven by the DMA. Each block in the system is a memory-mapped peripheral to the controllers, and has a series of addresses reserved for configuration and output data. Each block can be simultaneously accessed by either bus assuming that no write conflicts occur. Peripheral blocks each contain an address decoder to determine the destination of bus data.

Each block in the system has a configuration register containing bits for reset, clock gating, and power-gating. Using this, blocks can be individually controlled and put into a variety of states. The LCU has the capability to override the reset and power gate functionalities at the block level, allowing for an immediate system shutdown in the event there is a reduction in available system energy. Most

peripherals contain three individual power domains to conserve power during runtime while maintaining basic system functionality. All configuration registers in the system are powered on to maintain the block state, while the decoders can be power-gated using the LCU. The core logic of each block can be turned on/off using the configuration registers.

The SoC also contains the following blocks:

LCU
The lightweight control unit (LCU) is a light-weight, always-on custom MCU that is capable of data, node and processing flow control. This lower power LCU is capable of controlling the whole system without the openMSP430 through the openMSP bus. Its custom ISA and use of interrupts greatly reduces the size of the instruction program and therefore the instruction memory, thus resulting in a system wide power savings.

DPM
The digital power manager (DPM) is always on power manager of this energy harvesting node. In this DPM, the user has the ability to program both the thresholds and the operating mode control bits, thus enabling the programmer to prioritize functionality as the amount of energy is waning and utilize different power modification techniques that are local to the block. Additionally, we provide additional flexibility by sampling and digitizing the energy on the capacitor through an ADC or a temperature/PVT intolerant ring oscillator.

Clock Module (Leveraged by the openmsp430)
The digital clock module receives the clock from the ADPLL and gives the ability to the LCU or the openMSP430 to control the frequency of operation and reset for the entire system. This is useful for debugging purposes from the openMSP430 UART interface.

ADPLL
The system clock consists of a novel dual-loop ADPLL architecture that eliminates the divider – resulting in extremely low power consumption without performance degradation. This 187kHz to 500kHz ADPLL consumes 300-600nW from a 0.5V VDD, has a jitter <0.1% and occupies 0.07mm^2 in a 0.13µm CMOS process. The entire ADPLL was implemented using standard digital design flows and automatic place and route (APR). Moreover, an integrated crystal oscillator (31.25 kHz) is included and serves as the reference for the PLL.

SRAM
The system features four 2 KB memories: an RX buffer, TX buffer, LCU instruction memory, and MSP instruction memory, as well as a single 4 KB data memory. In order to ensure reliable operation at 0.5V, the 8T bitcell is used as the core storage device. Because this bitcell is still susceptible to half-select instability in column-muxed designs, a read before write scheme is implemented. During a write, the entire selected row is first read through the 2T read buffer and internally latched during the first half of the cycle. The latched data is then written back on the negative edge of the clock, along with the new data word. The memories are partioned into 1 KB banks, which can be independently power gated if they are not needed.

Power Management
We have included an integrated energy harvesting and power management circuit which achieves 63.6% end-to-end peak efficiency while delivering high load current (3-5mA). The system can harvest

power from a DC input source like a thermoelectric generator (TEG) or photovoltaic cell (PV). The boost converter can harvest energy from as low as 10mV and charges Vcap to 1.5V. An integrated Maximum power point tracking (MPPT) scheme tunes the input impedance of the boost converter to extract maximum energy from the ambient source. A Single-inductor multiple output (SIMO) DC-DC converter regulates the Vcap to a 1.2V and 0.5V supply, which are leveraged by the microcontroller in active, sleep and deep sleep modes. Once the Vcap is charged, the SIMO regulates the voltage on Vcap and provides a well regulated and stable 1.2V and 0.5V output at high load currents of 3-5mA.

Transceivers:
The SoC also includes a narrow band receiver, an ultra wide band transmitter, and a wakeup receiver for RF connectivity in its dual use applications.

FIR
A four-channel, 16-bit FIR filter, with each channel having up to 16-taps. The number of coefficients, number of active channels, and number of parallel filters are programmable. Each channel can be independently clock gated when not in use.

Histogram
This block can construct up to three histograms of data over time. The bin thresholds and number of active bins are programmable. Each histogram can contain up to 32 bins. One histogram has the option of only recording data when it's above a certain threshold or stopping data acquisition once a certain number of events have been recorded.

DMA
For this platform, the bulk of data needs to be transferred between the various peripheral blocks and the on-chip memories. This data transfer is more efficient when it can be done without constantly engaging the bus one controller. The DMA is a two-channel bus two controller. It can be configured using either of bus one's controllers to complete transfers between data in the peripheral memory space. Programmable options for each channel include source address, destination address, the number of transfers, the transfer type (e.g. peripheral to peripheral or memory to peripheral), intervals between each transfer, and the transfer mode (static, increment, decrement, or round robin). In the event of a peripheral access conflict (e.g. write conflict), the bus one controller takes priority and the DMA re-attempts the transfer after *NUM_TRANSFERS+1* clock cycles. Both channels can be active at once, but channel one takes priority in the event of a conflict.

SPI
The SPI master is a modified version of the Open Cores Simple SPI [http://opencores.org/project,simple_spi] with additions for bus interfacing and an added slave select signal. At minimum, it is a 3-wire protocol. It includes a 128 entries deep read and write FIFO, options for interrupts, enables, clock phase, and clock polarity. Data can be moved from a memory-mapped register to write to the FIFO before transmission, and data can be read through a memory-mapped register from the read FIFO after transmission is complete.

FFT/IFFT
This is a 16-pt, complex FFT and IFFT. This block repurposes a single radix-2 butterfly per clock cycle and uses in-place memory addressing to reduce the memory requirements.

Timer
This includes two, independently controlled timers for general purpose use. The block can be programmed to increment or decrement, rollover, and have a divided-down clock input for increased range. Each timer has an interrupt tied to the LCU and MSP when the timer has finished.

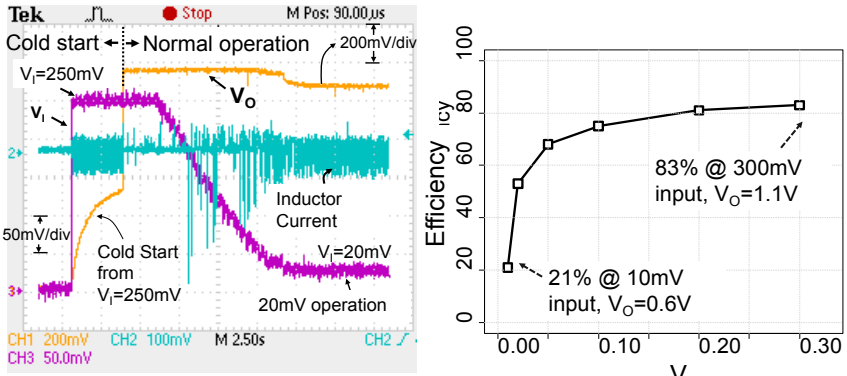
OMSP Multiplier
This is the peripheral multiplier that came with the openMSP430 block. It can be configured to do an unsigned or signed multiplication/MAC.

CORDIC
The CORDIC block provides the ability to calculate functions as sine, cosine, atan, square root, hyperbolic sine/cosine, exponential and natural logarithm, required by BSN applications such as arrhythmia classification, auscultation aids or gait speed estimation. The block has a 16-bit instruction, where four bits are used to specify the function to calculate and the remaining 12 bits are the data. A decoder uses the 4-bit instruction to set up the control logic to perform a circular, linear, or hyperbolic calculation in vectorial or rotational mode, while the main datapath of adders and shifters are re-used.

OMSP
We included the OpenMSP430 core, which is compatible with the Texas instruments MSP430 microcontroller family. We write and compile code generated by the MSP430 tool chain and are able to program it via the UART interface. This block can be configured by the LCU as the main controller or can act as a bus peripheral that is used only when ALU functionality is required.

The design of the SoC integrates over two dozen blocks including two microprocessors, four memories, and four radios. System level tests are ongoing, with the latest chip hardware only becoming available in August, but we have several significant results from components to report.

Designed for thermoelectric energy harvesting in 130nm CMOS, the boost converter reduces the achievable input voltage by 50% over the best prior art to 10mV, which allows wearable body sensors to continue operation with thermal gradients below 1°C. The design uses a peak inductor current control scheme and duty cycled, offset compensated comparators to maintain high efficiency across a broad range of input and output voltages. The measured efficiency ranges from 53% at V_I=20mV to a peak efficiency of 83% at V_I=300mV. Figure 2 shows measured waveforms and efficiency numbers for the boost converter.



a) Boost converter operation from cold start to 20mV V_I

b) Efficiency variation with V_I

Figure 16. a) Boost converter cold-start from 250mV, normal operation from 250mV to 20mV V_I b) Measured efficiency of the boost converter with V_I.

This boost converter is combined on the SoC with a single inductor, multiple output (SIMO) DC-DC regulator that regulates 1.2V and 0.5V rails for the chip. Together, the blocks provide a complete power delivery solution for energy harvesting. The SIMO efficiency is in the 90+% range, and the end to end efficiency is best reported across the input range for harvesting. The boost converter further incorporates maximum power point tracking for harvesting from both thermoelectric generators (TEGs) and solar.

Figure 17 shows the detailed block diagram of the power solution on the SoC and measurements of the maximum power point for a COTS solar cell, the boost converter operating at the MPP from solar energy indoors, the regulated SIMO output rails running from harvested indoor solar power, and the V_{IN} voltage tracking the V_{MPP} to show correct MPPT operation.

The SIMO regulator supplies a 1.2V power rail that can be used to power the AFE chip in the NEMO system.

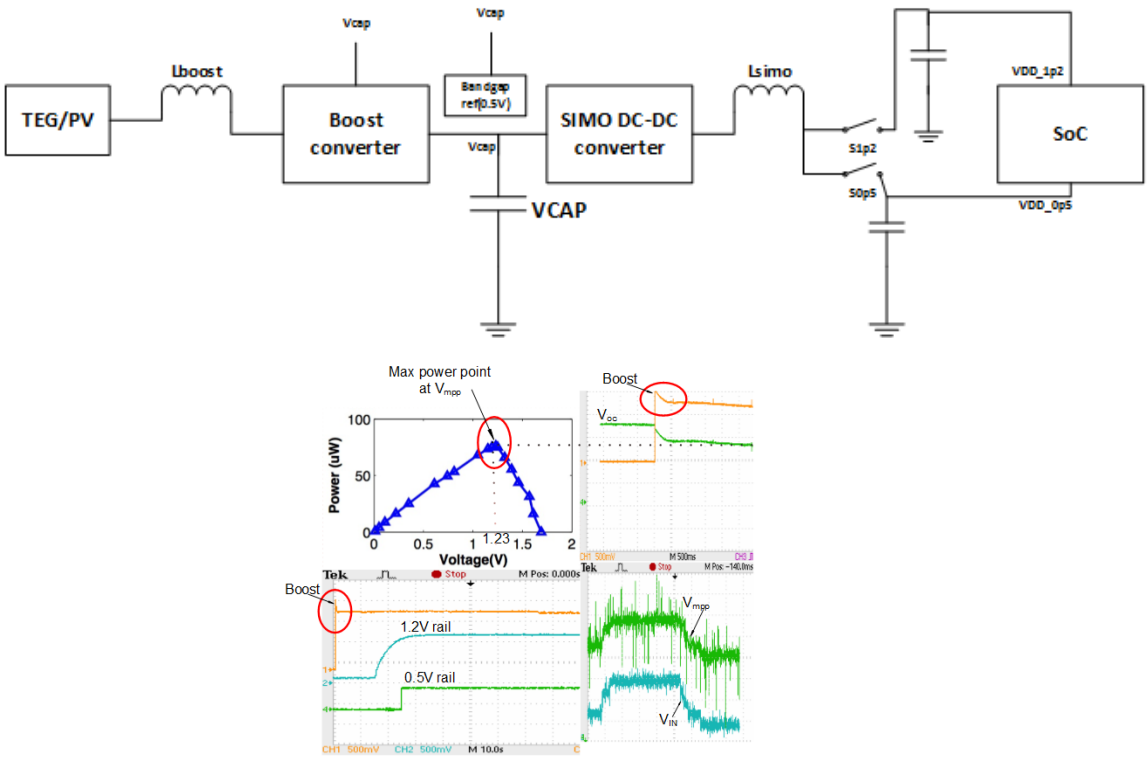


Figure 17. Full power delivery solution on SoC. Measured results showing correct startup, MPPT, and SIMO regulation.

Similarly to the design reported last year, the SoC supports dive profiling as described in Figure 18. The total digital power consumption of the chip is roughly 2 µW. When integrated with the AFE chip, the SoC will provide a continuous and very low power solution for depth and acoustic monitoring on deep diving whales.

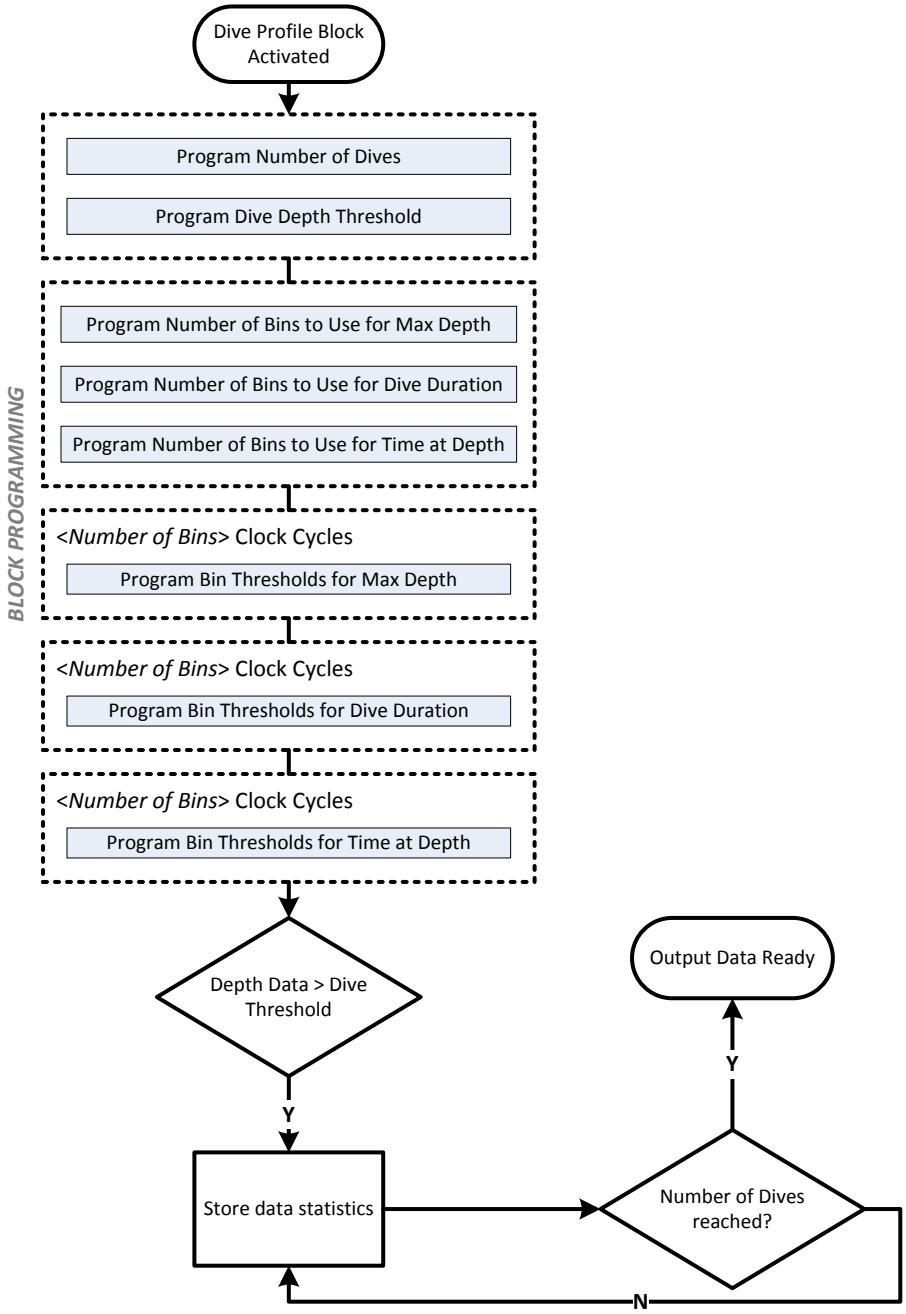


Figure 18. Dive profile functionality flowchart.

IMPACT/APPLICATIONS

The goal of this project is to develop a marine mammal tag to last for several weeks. This tag will allow data collection over much larger temporal scales (and therefore spatial scales) on deep diving whales and eventually smaller marine animals. The SoC-based NEMO tag will directly impact marine

mammal studies by allowing longer acquisitions. Also, the ULP processing that NEMO supports will expand data collection efforts to allow for automatic information extraction or reactive tag behavior (e.g. the tag can respond intelligently to specific identifiable events such as certain types of acoustic signatures or abrupt changes in typical dive behavior). The ULP consumption of the system will allow for future NEMO versions that use much smaller form factors, allowing for tagging of smaller marine species, such as harbor porpoise, which typically are not tagged with bioacoustic tags. Future versions of the tag may decrease power to the point that they can harvest ambient energy from their environment (e.g. a propeller) and provide near-perpetual sensing. The SoC based tags will dramatically improve the ability of the Marine Mammals and Biological Oceanography Program and of the US Navy to learn about marine animal behavior. Further, the SoC that performs data acquisition, customizable real-time signal processing, and storage and transmission of processed data will have dual use in a variety of other important application areas related to the US Navy's mission, including environmental and medical sensing, autonomous underwater vehicles (AUVs), and unmanned aerial vehicles (UAVs). The PIs will seek to transfer the SoC resulting from this research to the DoD, likely by partnering with a company capable of full-scale IC manufacturing and quality control.

RELATED PROJECTS

Two projects on body sensor node development are synergistic with the low power IC development in the mammal tag project. We hope to leverage low power blocks generated by students working on the NSF body sensor awards to improve the design of the marine mammal tag SOC.

"NSF Nanosystems Engineering Research Center for Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST)"
Source: NSF nano Engineering Research Center (nERC), subcontract with NCSU

"CSR:Small:Collaborative Research: Rethink Recharging – Wireless Batteryless SoCs to Power the Edge of the Cloud" Source: NSF CNS

PUBLICATIONS

The following publications did not directly arise from deliverables for this award, but they represent related work that is likely to be included in the final system on chip for the marine mammal tag.

1. S. N. Wooters, Y. Zhang, J. Bolus, B. H. Calhoun, and T. Blalock, "A 0.3 nJ/sample Temperature Sensor for Low-Power Wireless Biomedical Systems," Journal of Low Power Electronics and Applications (JLPEA), 2014. (under review)
2. J. Bolus, B. H. Calhoun, and T. Blalock, "39 fJ/bit On-Chip Identification of Wireless Sensors Based on Manufacturing Variation," Journal of Low Power Electronics and Applications (JLPEA), 2014. (accepted)
3. A. Banerjee and B. H. Calhoun, "An Ultra-Low Energy Subthreshold SRAM Bitcell for Energy Constrained Biomedical Applications," Journal of Low Power Electronics and Applications (JLPEA), Vol. 4, No. 2, pages 119-137, May 2014.
4. A. Klinefelter and B. H. Calhoun, "A Reduced-Memory FIR Filter Using Approximate Coefficients for Ultra-Low Power SoCs," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2014.

5. A. Shrivastava, D. Wentzloff, and B. H. Calhoun, "A 10mV-Input Boost Converter with Inductor Peak Current Control and Zero Detection for Thermoelectric Energy Harvesting," IEEE Custom Integrated Circuits Conference (CICC), 2014.
6. A. Shrivastava, Y. K. Ramadass, S. Khanna, S. Bartling, and B. H. Calhoun, "A 1.2μW SIMO Energy Harvesting and Power Management Unit with Constant Peak Inductor Current Control Achieving 83-92% Efficiency Across Wide Input and Output Voltages," Symposium on VLSI Circuits, 2014.
7. Y. Zhang and B. H. Calhoun, "Fast, Accurate Variation-Aware Path Timing Computation for Sub-threshold Circuits," International Symposium on Quality Electronic Design (ISQED), 2014.

HONORS/AWARDS/PRIZES

NA