Amendment Number 0001

Broad Agency Announcement 11-020

"Protection of Electronics Systems"

The purpose of Amendment Number 0001 is to provide answers to questions received under BAA 11-020, entitled "Protection of Electronics Systems," and provide additional information as follows.

Q#1: With regard to Research Topic (1) in ONR BAA 11-020, will the development of new types of non-volatile memory be considered, or does Research Topic (1) only refer to existing COTS memory?

A#1: The BAA states, "1. New Approaches to Memory Erasure - Technologies are sought for completely and irreversibly erasing data stored in non-volatile memory. ... It is desirable that the erasure technology work with current memory technologies, though erasure technology that works with other memory technologies will be considered. … "

New types of non-volatile memory capable of complete and irreversible erasure will be considered. However, erasure technologies that work with current memory technologies would be more desirable.

Q#2: Regarding the above referenced BAA, part 4: In the fourth part, ONR scientists want industry to develop ways to design and install physical unclonable functions (PUFs) in field-programmable gate arrays (FPGAs) to authenticate these FPGAs and generate volatile keys for advanced encryption and decryption. What are the restrictions, if any, as regards non-US company technology being employed? Would it be acceptable to this program if the primary work was carried out by the non-US engineers, or would it be necessary to use US citizen/US-based engineers, with the work being carried out in the US?

A#2: Due to security and export control restrictions, the work under this BAA research topic will be restricted research. It would not be acceptable if the work was carried out by the non-US engineers. It would be necessary to use US citizen/US-based engineers, with the work being carried out in the US.

Q#3: In topic 4, it is stated that ONR seeks "reliable intrinsic Physical Unclonable Functions (PUFs) in FPGAs"; does "in" refer to in-silicon implementation of dedicated PUF structures and/or the corresponding logic to evaluate one, or does it mean "in the user design programmed into the configurable logic"? Correspondingly, the authentication aspect of this topic elicits a similar question: Is the goal to authenticate with an interface exposed in the underlying silicon, or with the design in user-logic?

A#3: The second approach ("in the user design programmed into the configurable logic") is desired since it can be applied to unmodified commercially available FPGAs. The first approach ("in-silicon implementation of dedicated PUF structures") would require custom fabrication.

Q#4: Is there any means to vet one or more potential proposal directions to determine whether they align with the spirit of the BAA, or is whitepaper submission the only available vetting process?

A#4: The only communications permitted after the BAA was posted and prior to the whitepaper submission date are formal technical questions submitted by email to the POCs listed in the BAA, which are answered in the form of amendments to the BAA.

Q#5: Concerning Topic 1 of the Protection of Electronics Systems Discovery and Invention Program (BAA 11-020), can you comment on the preferred form(s) of non-volatile memory? For example, is standard flash memory the primary data storage medium of interest? In some contexts, magnetic media such as standard hard drives or micro-drives are considered non-volatile memory. Is that so in this program?

A#5: Solid-state non-volatile memory is desired. Non-solid-state, non-volatile memory, such as spinning drives, is not desired.

Q#6: I would like to know if there is any information or publication on the types of details you are looking for in the last three required sections of the white paper, That is: Future Naval Relevance, Operational Naval Concept and Operational Utility Assessment Plan. Please also let me know if there are any examples I could look at.

A#6: No additional information is available beyond the descriptions already contained in the BAA:

"Future Naval Relevance: A description of potential Naval relevance and contributions of the effort to the agency's specific mission.

Operational Naval Concept: A description of the project objectives, the concept of operation for the new capabilities to be delivered, and the expected operational performance improvements.

Operational Utility Assessment Plan: A plan for demonstrating and evaluating the operational effectiveness of the Offeror's proposed products or processes in field experiments and/or tests in a simulated environment."

Q#7: On page 6 of the announcement, there is a statement regarding a 35% limitation of indirect costs. We are seeking clarification on this statement. Our primary question is your definition of indirect costs. We have more than one pool of costs that are applied to a project over and above costs incurred specifically for the project. Our pools are (1) Fringe taxes and benefits pertaining to our work force, (2) Engineering overhead, which include a proportional charge for facilities and supervision costs, and (3) G & A, which is a proportional charge for our company's ongoing administrative, bids and proposals, selling expenses, etc. We believe that these pools are common to most if not all companies. Which of the above pools are included in your definition of indirect costs?

Second, does the limitation mean 35% of the total proposed costs or 35% of the direct costs incurred on this project? The wording of the statement would seem to point to the former – 35% of the total costs proposed.

Our last question relates to the timing of this limitation. We have submitted a number of BAA white papers and proposals, and have been awarded and performed one BAA based contract. This is the first time that we have encountered such a statement of limitation on indirect costs.

A#7: Part 1: This limitation is no longer applicable.

Q#8: Part 1: For Research Topic #2, is ONR looking for multi-chip chip-scale packages that essentially rely on chip stacking, or the ability to scale to larger modules containing many chips laterally and vertically stacked and the related passives in a 3D highly dense format?

Part 2: In a related question, what is the difference in Research Topic #2 and Research Topic #3? It seems that #2 is a subset of #3 with the requirements of #2 repeated in #3. #3 requires a FPGA, is this also what you are looking for in #2 or is #2 more of a system in a package?

Part 3: What is the upper frequency limit that the packaging technology should address?

A#8: Part 1: Either.

Part 2: Research Topic #3 is for the development and build of a prototype secure processor system that utilizes 3D packaging. Research Topic #2 is for research and development of technologies that address current areas of concern associated with 3D packaging such as cooling, EM interference, susceptibility and emissions.

Part 3: The upper frequency limit that should be addressed is 45 GHz. This is based upon the upper frequency limit identified in MIL-STD-464.