# Naval Research Reviews

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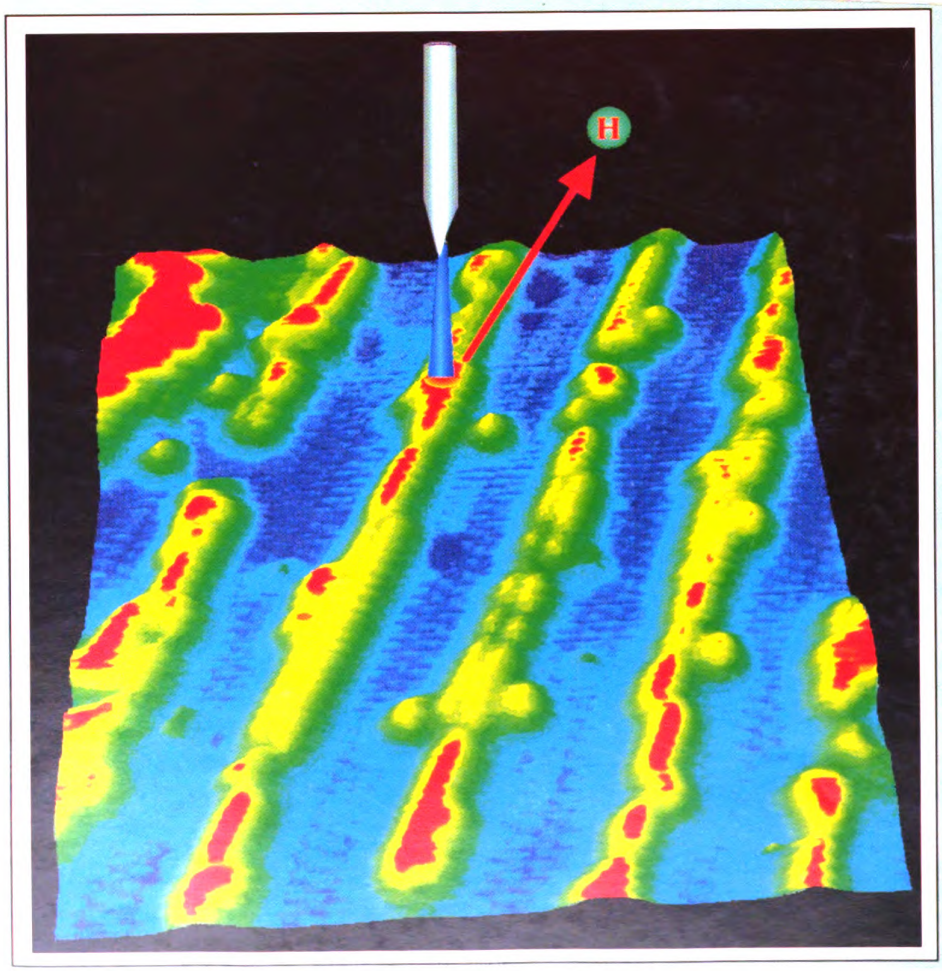
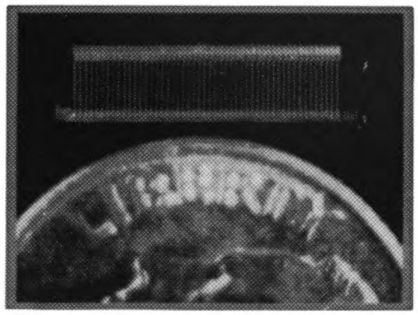



## Scanned Probe Lithography

# Array of 50 Cantilevers with Integrated Sensors & Actuators






Quate Group, Stanford University

The figure at the left is a photograph of a 1-cm-long array of 50 cantilevers. A dime is included in the picture for scale. The figure at the right shows that each cantilever has its own integrated sensor and actuator so that it can be controlled independently. The spacing between the cantilevers is 200 μm. These arrays are being used by the Quate group at Stanford University (see last article in this special issue) to demonstrate the practicality of scanned probe lithography.

# Naval Research Reviews

**Office of Naval Research**
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## Articles



## Departments





**About the cover**

This figure shows a scanned probe creating a lithographic pattern consisting of lines which are only one or two atoms wide. The surface is single crystal silicon, specifically Si(100), whose dangling bonds have been terminated with atomic hydrogen. The resultant monohydride layer serves as a resist in the lithography process. The hydrogen is locally removed by 3 V electrons from the scanned probe tip. The red regions are where single Si atoms have been exposed; the yellow regions correspond to exposed Si dimer pairs. This figure was provided by J. Lyding, University of Illinois, and these results are discussed more fully in his article in this issue.

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# Foreword

*by Dr. Richard G. Brandt, Guest Editor*
*Office of Naval Research*

The scanning tunneling microscope (STM) was invented in 1982, and it immediately opened up a new era in surface science by providing atomic-resolution images of conducting surfaces. The inventors of the STM, G. Binnig and H. Rohrer, were awarded a Nobel prize in 1987 in recognition of this major advance. The atomic microscope (AFM) was invented in 1986 by G. Binnig, C. Quate and C. Gerber, and it provided this same capability for non-conducting surfaces. The scientific literature of the late 1980s and the early 1990s is filled with numerous examples of breakthroughs in scientific understanding enabled by the invention of these scanned probe (STM, AFM and related) techniques. The Office of Naval Research (ONR) supported some of these early scientific efforts and supported the development of these new experimental tools.

Although most of the attention was focused on surface science applications in the early years following the invention of the scanned probe, it was apparent to many people that the most significant payoff from these inventions would result from the ability to manipulate atoms on surfaces to create nanometer-scale structures. I specifically recall a conversation I had with Cal Quate shortly after his invention of the AFM in 1986 in which he shared his vision of fabricating nanoelectronic circuits using these techniques.

In response to these science and technology opportunities and also the payoff potential of nanoelectronics for the Navy, the focus of the ONR program on surfaces and interfaces was shifted to nanofabrication and characterization of nanostructures. Similarly, the strong in-house program at the Naval Research Laboratory (NRL) aimed at developing and exploiting scanned probe techniques was expanded to include an emphasis on nanolithography for nanoelectronics.

A suitable nanofabrication technique is a necessary ingredient for the development of nanoelectronics. The Navy has a vital interest in nanoelectronics because of the expected performance advantages which include higher speed and lower power dissipation with a significant reduction in size and cost. These performance improvements will enable major new system capabilities. With this new focus, ONR and NRL scientists continued working together to promote programs directed towards scanned probe lithography. These efforts culminated in an ONR-sponsored University Research Initiative (URI) begun in 1992 which was specifically directed towards developing and understanding scanned probe techniques applicable to nanometer sized electronic structures. This URI fostered close interaction between NRL scientists and their academic counterparts, and these beneficial interactions are continuing.

The authors of this special issue are all pioneers in the field of scanned probe lithography. Their work has been supported by ONR, DARPA and other agencies. The first article is by Christie Marrian, who is Head of the Nanoelectronics Processing Facility at NRL. Christie provides an overview of the field of nanolithography. He describes the conventional approach to fabricating nanostructures which uses a high-energy electron beam to expose a resist layer, and he discusses the advantages and limitations of that approach. He shows that the use of low-energy electrons, supplied by a scanned probe, eliminates electron scattering in the resist and provides an easier way to achieve nanometer resolution. He also argues that pattern placement, i.e., the precision with which a feature can be positioned, is a more significant problem than resolution and describes an NRL approach to this problem. An ONR Small Business Innovative Research project is also addressing this problem by developing an inexpensive optical-based positioner capable of 5 nm repeatability over an entire silicon wafer. (This SBIR project is described in a Research Note at the end of this issue.) Christie mentions the issue of throughput which is a limitation of both high energy electron beam lithography and scanned probe lithography. Both techniques expose a single pixel at a time, and, because of this serial exposure, the processing speed is relatively slow and unacceptable for manufacturing applications. The final article in this series describes work in progress which significantly increases throughput in scanned probe lithography.

In the second article Eric Snow, Paul Campbell and Keith Perkins of NRL describe their scanned probe technique and discuss how it has been used to fabricate novel nanoelectronic devices. They utilize an AFM with a conducting tip. The feedback loop of the AFM keeps the tip floating over the surface by maintaining a very small constant force; the exposure process is independently controlled via a voltage applied between the conducting sample and tip. All exposures are performed in a controlled ambient environment rather than under high vacuum conditions. In some of their work they are exploring the use of self-assembled monolayer films as resists and imaging layers. However, the bulk of the paper describes the modification of surfaces directly with an AFM. An oxide is grown beneath the tip and used as a resist in subsequent processing steps. The oxide is formed via an electrochemical reaction with water vapor in the ambient. Using this technique on silicon they have demonstrated operating devices with critical dimensions as small as 30 nm. They have succeeded in fabricating feature sizes less than 1 nm in metal structures by a novel extension of this technique in which they anodize through a very thin metal wire while monitoring the conductance of the wire. In this way they can reduce the cross section of the wire and lower its conductance, finally reaching the lowest possible non-zero value where the conductance is due to a single atom point contact. These techniques are being used to fabricate novel nanoelectronic devices. They

plan to fabricate and evaluate a metal/metal-oxide transistor in which the metallic source and drain regions are isolated from the conducting channel by oxide tunnel barriers formed by the anodic process described above. This same device concept, but fabricated in silicon with silicide barriers instead of metal/metal-oxide, is also being pursued by John Tucker of the University of Illinois as a DARPA-funded extension of the URI project on nanolithography.

Joe Lyding has been the leader of the ONR URI nanolithography program since its inception in 1992. In his article he describes the accomplishments of this program. One of the program goals is to reach the ultimate limits of lithography. This can only be achieved by operating in ultrahigh vacuum (UHV) where surfaces are stable at the atomic level for long periods of time. Lyding, Tucker and coworkers operate in a sophisticated UHV system containing several chambers for sample preparation, exposure, and analysis. The standard sample is single-crystal Si(100) which is cleaned and then passivated with atomic hydrogen. The hydride layer serves as a resist which is a single atom thick. The exposure tool is a UHV-compatible STM. Under normal scanning conditions the STM does not perturb the hydrogen-passivated silicon surface. However, by increasing the voltage between the tip and the sample, hydrogen can be desorbed. They have performed a series of measurements to fully characterize the desorption process as a function of tip voltage and electron dose. Lithographic patterns have been produced with linewidths as small as 1 nm. The illustration on the cover of this issue shows the narrowest lines obtained which are only 1 or 2 atoms wide. The next step in the lithography process is to convert the exposed regions into another useful form. Lyding, Tucker and coworkers have demonstrated that the hydride resist in the unexposed regions is reasonably robust and that regrowth of oxides, nitrides and metals can be accomplished in the exposed regions by selective chemistry techniques. In addition to these major advances in the field of nanolithography, the URI produced another, unexpected breakthrough. As a result of these fundamental studies of hydrogen desorption and comparison studies on deuterium desorption, Joe Lyding and his URI colleague Karl Hess (featured under Profiles in Science in this issue) speculated that deuterium might be much more effective than hydrogen in passivating dangling bonds at buried interfaces in silicon MOSFET devices, thereby overcoming hot electron effects which result in device degradation. An experiment was performed with a colleague at Lucent Technology, and the result was a dramatic improvement in operating lifetime by a factor of 10 or more. This improvement has now been confirmed by many other industrial groups. This breakthrough translates into significant payoffs for the Navy. The new long-life integrated circuits enabled by this discovery will find application in satellite systems and other systems such as avionics where repair access is difficult, thereby lowering maintenance costs and improving affordability.

The final article is by a research group at Stanford University led by Cal Quate. This group is addressing the critical issue of throughput. For scanned probe lithography to be a viable manufacturing technique, an entire wafer must be processed in a reasonable time period, no more than several minutes. This cannot be accomplished by a single scanning tip. The approach being developed is to use an array of independently controlled AFM tips with each tip scanning at the highest possible rate. Their design calls for a linear array of several hundred tips with each tip scanning at a rate of 25 mm/sec. The scan speed of a typical AFM is about 0.2 mm/sec which is limited by the properties of the bulk piezoelectric actuator that positions the tip. The Stanford group has made a major advance in scan speed by integrating the actuator onto the cantilever structure. With the integrated actuator they have been able to achieve scan speeds of 3 mm/sec. In a typical AFM, cantilever deflection is measured by an optical reflection technique using a laser beam and a photodiode detector. The Stanford group has developed a nonoptical technique which uses a piezoresistive sensor integrated onto the cantilever to measure deflection, and using these integrated actuator/sensor cantilevers they have fabricated and tested 2- and 4-element arrays of independently controlled tips. The circuitry to control arrays much larger than 4 elements becomes complicated, and an alternative optical readout technique is also being investigated. This requires fabricating each cantilever into the shape of interdigitated fingers and illuminating the array with a single laser beam; cantilever deflection is determined by measuring the intensity of diffraction spots from each cantilever. An array of photodiodes is required, one per cantilever, but such photodiode arrays are readily available commercially. Using these several approaches the Stanford group is determined to achieve their goal of high speed array operation. In parallel with these array efforts they are also exploring suitable resists for scanned probe lithography. They have shown that a thin deposited layer of amorphous silicon, which can be augmented by a metal underlayer, is a robust resist for nanolithography and that pattern transfer can be accomplished using this resist. Thin organic polymer resists of the type described in Christie Marrian's article are also being evaluated. Uneven surface topography causes the resist layer to have nonuniform thickness, resulting in variable linewidth under the usual constant voltage exposure conditions. This problem has been solved by implementing an additional feedback loop which maintains a constant exposure current independent of resist thickness. Using this modified AFM exposure tool with two feedback loops (one to maintain constant force and the other to maintain constant exposure current), they have succeeded in fabricating operational MOSFET devices with an effective channel length of 100 nm which is a convincing first step in their goal to fabricate nanoelectronic devices.

This series of articles shows that remarkable progress has been made in developing scanned probe nanofabrication

techniques. The dream of a decade ago has become reality. Progress has been achieved on many fronts -- lines one or two atoms wide have been defined, single atom point contacts have been controllably fabricated, robust high resolution resists have been developed, nanoscale patterns have been transferred, working devices have been demonstrated, and novel nanoelectronic devices are being investigated. The serious concern about processing speed and throughput is being vigorously addressed, and there has been significant progress. ONR and NRL have played a major role in the development of this field and have either sponsored or contributed to most of the advances described in these articles. Proof-of-principle demonstrations of scanned probe instrumentation for nanofabrication are already impacting nanoelectronics and microelectronics R&D. Looking to the future, the potential for the field is particularly exciting.

## Biography

Dr. Richard G. Brandt graduated from Yale University with a Doctorate of Philosophy in Physics. He is a Program Officer in the Electronics Division at the Office of Naval Research, managing a program which addresses surface and interface issues that affect the performance of electronic materials and devices. He has a strong interest in nanofabrication and nanocharacterization. Before ONR he worked in academia and in industry.

# Nanolithography

*by Christie R.K. Marrian, Nanoelectronics Processing Facility, Naval Research Laboratory, Washington DC*



## Abstract

The rapid development of the field of nanometer science and technology has been driven to a large part by our increased ability to fabricate and characterize structures with nanometer scale dimensions. The challenges inherent in the fabrication of nanostructures with atomic-scale precision have led to the development of a scientific discipline with an intellectual content of its own. Lithography, the definition of an arbitrary pattern in a sample or a sacrificial layer on that sample, is an integral part of this scientific endeavor. This paper reviews some of the current challenges in improving the accuracy and size of features formed in a nanolithographic process. The emphasis is 'conventional' nanolithography where high energy focused particle beams are use as the lithographic tool. The advantages of a proximal probe approach to nanolithography are highlighted here and, in more detail, in the following papers in this issue.

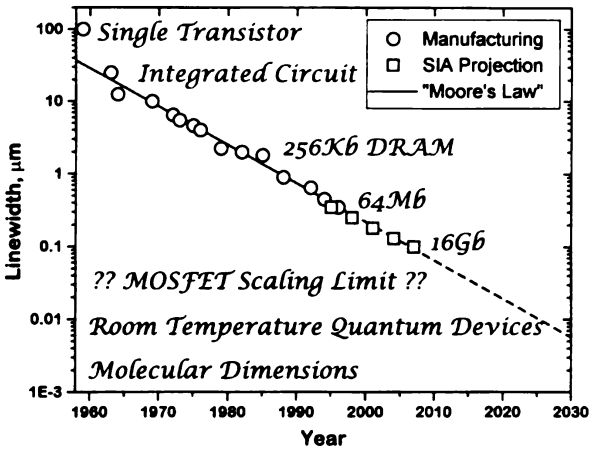
## 1. Introduction

### 1.1 Length Scales in Microelectronics

Current volume manufacturing of silicon based integrated circuits (such as memory chips or microprocessors) requires the definition of features with critical dimensions (CDs) of ~350 nm. Within the next year or so, integrated circuits with features down to 250 nm in size will appear in the market place. Furthermore, each circuit will contain hundreds of millions of such features over area of a square inch or so. If such a circuit were enlarged so that the minimum features were the dimension of a human hair (25 μm), it would be about 8 square yards in size. The microelectronics industry has been pursuing an aggressive miniaturization of CDs since the fabrication of the first planar transistor in

1959. This phenomenon was first spelled out by Gordon Moore, one of the founders of Intel, in 1975 when he remarked that feature sizes in volume manufacturing had decreased by about 30% every 3 years.[1] This trend has continued ever since (see figure 1) and is often referred to as Moore's law. Also included in figure 1, are the extrapolations of Moore's law which have been detailed by the Semiconductor Industry Association (SIA) in their Lithography Roadmap.[2] Indeed the prosperity of the microelectronics industry is closely linked to its ability to stay on this projected path. Looking further out into the future one can see that the point will eventually be reached when down scaling of existing silicon based metal-oxide-semiconductor transistor (MOSFET) technology will no longer be possible. The MOSFET scaling limit is currently believed to be 30-50 nm. Below this limit the physical phenomena which are dominant in the nanometer size regime become candidates for a device technology from which computationally functional circuits could be fabricated. These physical processes are now the subject of intense research and development in academic, corporate and government, including Navy, laboratories.[3]

**Figure 1**
*Trends in volume manufacturing for DRAM integrated circuits. This type of plot is often referred to as Moore's Law.*




## 1.2 Length Scales for Nanoelectronics

As described above, downscaling of silicon based MOSFETs is currently expected to be possible to below 50 nm. Researchers have identified a number of physical phenomena on which to base a future device technology to replace the MOSFET. These mechanisms include Coulomb blockade, resonant tunneling, quantized conductance fluctuations and electron phase effects. To illustrate the lateral feature sizes required, an example based on the Coulomb blockade will be described. (Similar dimensions are required for resonant tunneling and still smaller for the other mechanisms.) The Coulomb blockade arises because electric current is the result of the flow of discrete particles (i.e., electrons). If one makes a capacitor small enough, the energy needed to add an additional electron ($q^2/C$, where q is the charge of an electron, C is the capacitance) is significant. To be useful as an electronic switch, 'significant' means that the charging energy must be much greater than the thermal energy of the electron which, at room temperature, is 25 meV. A 'back of the envelope' calculation shows that this requires a capacitor with lateral dimensions of about 10 nm, i.e., some 30 atomic diameters.

## 1.3 Department of Defense Needs for Micro- and Nanoelectronics

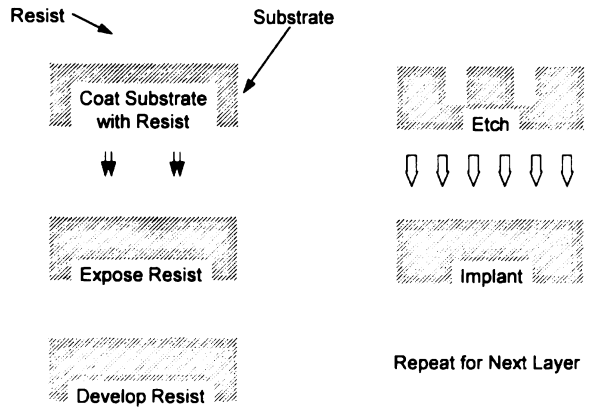
Even a casual glance at a Navy installation reveals the tremendous use that is made of state-of-the-art electronics for computation and information processing. For example, weapon systems and ship-borne navigation and defense systems all depend on large amounts of data being processed in real time for personnel and ship protection, targeting and electronic, as well as conventional, warfare. Thus there is a generic need for state-of-the-art electronics technology throughout the nation's defense organizations.

In addition, and perhaps more importantly, the Navy requires unfettered access to numerous specialized components based on advanced electronic materials. These include multi-spectral imaging systems, ultra high density data storage, biological and chemical sensors, analogue electronics and high bandwidth radio frequency devices. Unfortunately, such components will not necessarily be available from the private sector. Furthermore, the performance of all these components will benefit from decreased critical dimensions. Integration this type of advanced electronics into military systems will result in an increased awareness of, and protection from, an adversary along with an ability to strike surgically at the most critical elements of an antagonist's infrastructure.

## 1.4 Lithographic Choices

A schematic view of the microfabrication process is shown in figure 2. A sacrificial material (resist), whose physical or chemical properties change upon energetic irradiation, is applied in a thin (<100 nm for nanolithography) film to cover the sample to be patterned. A pattern is then defined in the resist material by a spatially selective exposure with some form of energetic radiation, such as photons, electrons or ions. This step is referred to as lithography. The latent litho-

**Figure 2**
*Schematic of a lithographic process which is applicable to the sub 100 nm regime if the exposing radiation has sufficient resolution.*




graphic image is transferred into a relief image in the resist film by a development step in which the exposed (unexposed) areas are washed away if the resist is positive (negative) tone. The lithographic pattern can then be transferred into the substrate by a process such as etching or implanting (as shown). Alternatively, material can be grown or deposited onto the substrate using the pattern in the resist as a template. To fabricate a complete integrated circuit, the process is repeated several times with each layer carefully aligned to the previous one.

Manufacturing lithography is dominated by projection optical lithography and will continue to be so for at least six years. A mask is fabricated representing the lithographic pattern. Then the entire pattern is projected onto the resist covering the workpiece. Thus a large number of pixels (a pixel is the smallest defined element of the lithographic pattern) are printed simultaneously, i.e., in parallel.

The need for ever smaller dimensions has been accommodated by a combination of increasing the numerical aperture of the illumination system and decreasing the wavelength of the illuminating radiation. Currently, features close to the size of the incident radiation are printed. Lithography for the next two manufacturing generations, with 250 nm and 180 nm CDs, are planned to be based on KrF ($\lambda$=248 nm) and ArF ($\lambda$=193 nm) excimer laser radiation. The choice for subsequent generations is not clear at this point, but the leading candidates have been identified by the SIA and include x-ray ($\lambda$<1 nm), soft x-ray ($\lambda$=14 nm) and projection electron beam lithography.[3] These lithographies are the focus of several research and development efforts sponsored by both the Department of Defense[4] (DoD) and Industry.[5]

Nanoelectronics research requires feature sizes well below that which are available from manufacturing lithographies. On the other hand, the throughput requirements are orders of magnitude lower because only a relatively small number (<1000) of devices or structures is required. This allows the use of a variety of serial (each pixel in a pattern is exposed sequentially) lithographic techniques. Lithography aimed at the sub 100 nm regime is usually referred to as nanolithography and is the subject of much DoD sponsored research. For example, the issue of resolution limits for a particular set of lithographic parameters requires a detailed understanding of the physical mechanisms of energetic particle-solid interactions. However, resolution alone is not sufficient for a viable nanolithographic technique. It is also essential to be able to define arbitrary patterns and to be able to place the pattern precisely at a desired location. Recent research in this area at the Naval Research Laboratory (NRL) is highlighted in the remainder of this paper and in the companion paper by Eric Snow, Paul Campbell and Keith Perkins.

# 2. Nanolithography With Electrons

A steered focused beam lithography is the preferred technique for nanolithography as well as mask making, prototyping and small scale production in present day microelectronics processing. The technology of choice is high energy e-beam lithography as a wide range of tooling is available and the requisite expertise is well documented in the literature.

Over the past decade or so, the search for techniques to increase resolution has followed two paths. First, the spot size of the e-beam tool has been decreased by improved focusing usually accompanied by increasing the energy of the electrons. As a result, commercial tools operating at 100 keV and converted transmission electron microscopes operating at several hundred keV have all been used to push the resolution of e-beam nanolithography. The second approach is to use extremely low voltages. Here the problems associated with electron scattering are avoided so the energy of the electrons can be deposited into a volume close to that defined by the spot size of the beam. The logical extension of this is to use essentially zero (<50 eV) incident energy. This can be achieved by using a scanning tunneling microscope to generate a spatially confined (although not focused) beam of electrons. These approaches are discussed in more detail in the following sections. Indeed efforts at improving resolution have been so successful that resolution is no longer the major problem associated with e-beam lithography except at the smallest dimensions (<30 nm). The chief problem for advanced prototyping and mask making with e-beams is the precision with which a feature can be positioned, i.e., pattern placement. To put the requirements of pattern placement in perspective, the accuracy with which a feature must be placed on a work piece is typically required to be less than 15% of the minimum feature size. Thus for 50 nm fea-

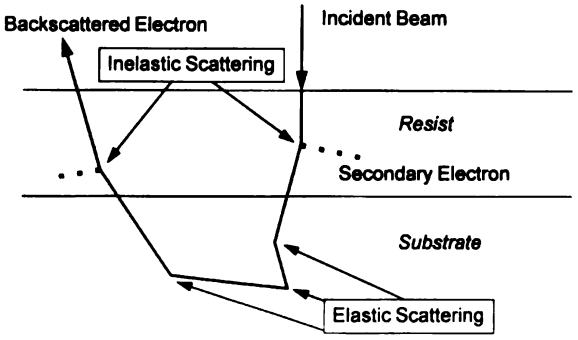
tures, a precision of 8 nm or ~22 atomic spacings is required. How such precision could be achieved is also discussed below.

## 2.1 High Energy Electron Nanolithography

### 2.1.1 Modeling of e-beam Lithography

Accurate modeling of electron scattering has become increasingly important as more reliance is placed on simulation to optimize e-beam lithography processes. The simulation approach is schematically illustrated in figure 3. Using a Monte Carlo approach, many ($>10^5$) electron trajectories are calculated and the energy deposition as a function of position from the point of incidence of the primary beam (the point spread function) is determined. Our recent work has investigated the importance of the various physical mechanisms which are incorporated in a Monte Carlo code. Specifically, we have studied the inclusion of inelastic scattering (i.e., the creation of fast secondaries) and the form of the elastic scattering cross section on e-beam lithographic spread functions. Previous work of this type has highlighted the issue of resolution limits in e-beam lithography[6] and/or curve fitting approximations to lithographic spread functions.[7]

**Figure 3**
*Schematic of Monte Carlo approach to calculating electron trajectories to generate lithographic spread functions.*




To compare the results from our Monte Carlo simulations with actual lithographic measurements, the feature size versus dose is calculated for a variety of patterns (dots, lines and gaps between two small pads). The point spread function is first integrated to give the line spread function, i.e., the energy deposited as a function of distance for an incident dose per unit length. The line spread function is then integrated to calculate the absorbed energy in a gap between two pads as a function of incident dose per unit area applied to the pads. The spread functions have been fitted to the experimental data using a parameter corresponding to the energy density absorbed in the resist which is required to expose the resist (this value is referred to as the 'energy threshold'). This has the effect of moving the spread function plots parallel to the dose axis in a plot of feature size versus dose. Studies of three different resist materials showed that the energy threshold is dependent on resist material (i.e., some resists are more sensitive than others). However, for a given resist, the energy threshold is independent of incident electron energy and the shape of the exposed pattern. This last point is illustrated in figure 4 which shows a comparison between experiment and simulation for zero (dot), one (line) and two (plotted as the magnitude of the error in the size of the gap between two pads) dimensional patterns in a thick resist film (1.45 μm) exposed with a 20 keV electron beam. The same value for the energy threshold fitting parameter was used for all three types of patterns.

In figure 4, the importance of secondary electrons is also illustrated. The dotted line is the line spread function generated when secondary electron creation is not included. Clearly the inclusion of fast secondaries improves the fit between experiment and simulation for features between 200 nm and ~2 μm in size. The same improvement in the fit for the dot and gap data is observed but has not been included in the figure for clarity.

**Figure 4**
*Comparison of simulation and experiment for dot, line and area patterns for a 1.45 μm resist film on silicon irradiated with 20 kV electrons. The solid lines represent the spread functions calculated when secondary electron creation is included. The dotted line represents the line spread function calculated when secondary electron creation is forbidden. The data for the area patterns is plotted as the magnitude of the error measured in the gap between two pads 100 by 200 μm in size. At low doses the pads are underexposed and the gap is larger than its nominal value (2.5 μm). At doses above ~13 μC/cm², the pads are overexposed the gap is smaller than its nominal value.*

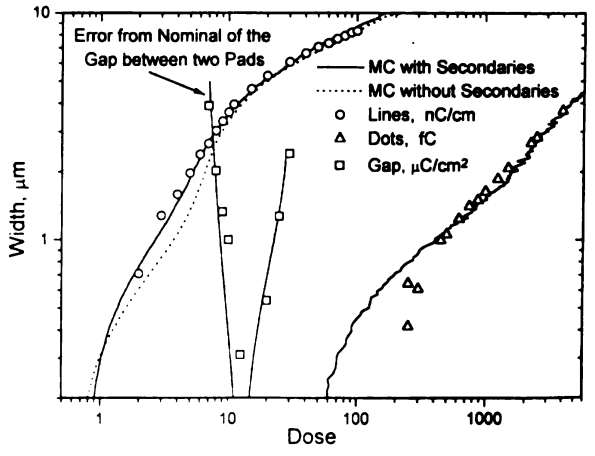


**Figure 5**

*Nanolithography of isolated line patterns in a 50 nm film of resist on silicon exposed with a 50 kV e-beam. The dotted line represents the line spread function calculated when secondary electron creation is forbidden. Note the improved fit between data and simulation when fast secondary creation is included.*

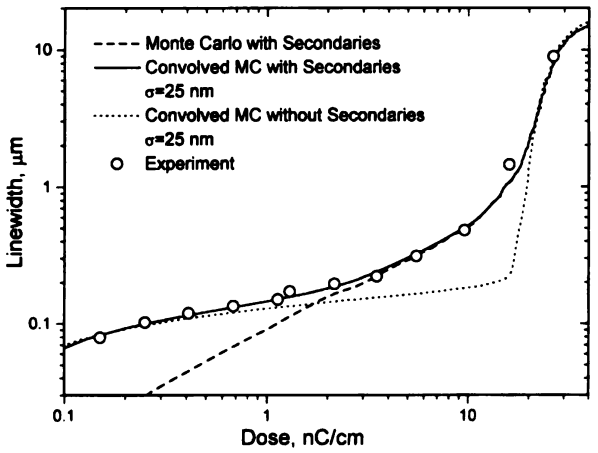
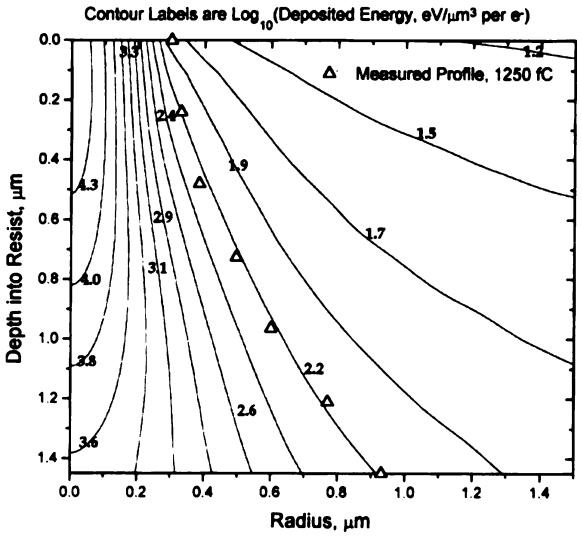



**Figure 6**

*Energy deposition through a 1.45 μm film of resist irradiated with 20 kV electrons. Contours of constant energy deposition (determined from our Monte Carlo simulation) are compared to measurements of the profile of a dot exposure in the same*




To achieve smaller feature sizes, a higher beam energy (e.g., 50 keV) and a thinner resist film (e.g. 50 nm) is required, figure 5. Here the effect of the fast secondaries in the 100 nm to 1 μm regime is clear. However, even with the inclusion of these secondaries, the simulation underestimates the observed feature sizes at the smallest (<100 nm) dimensions. The fit is improved by convolving the spread function with a gaussian to broaden the spread function at the smallest feature sizes. In this case, convolution with a gaussian of a standard deviation of 25 nm is required, which is significantly larger than the estimated 10 nm probe size. This issue is discussed further in the next section.

In addition to predicting the lateral extent of features as a function of the applied dose, the simulation can be extended to three dimensions, i.e., the profiles of the resist features can be predicted as illustrated in figure 6. Here contours of constant energy deposition are plotted down through a relatively thick resist film. The points represent measurements from a micrograph of a 1250 fC (~7.5 million electrons), 20 keV dot exposure of a resist film of the same thickness. Excellent agreement is seen between these points and the contour labeled 2.2 which corresponds to an energy deposition of $10^{2.2}$ (~160) eV/μm$^3$ per incident electron. For dot exposures less than 1250 fC, the resist profile becomes more vertical before exhibiting a pronounced undercut as shown in the contours labeled >3.1.

The ability to control the undercut in the resist profile has been utilized to fabricate sub micron sized apertures in a thin metal film using a lift-off process. (The alternative would require a plasma etch to define the apertures which would cause significant electronic damage to the underlying semiconductor.) This process has enabled some dramatic spectroscopic photoluminescence studies of single quantum dots here at NRL.[8]

## 2.1.2 Resolution Considerations

The lithographic performance of high energy e-beam tools is usually not determined by the size of the focused beam itself. While the mechanisms responsible are still the subject of much study, it is thought there are two processes at work. The first is associated with the resist material itself and is best illustrated in terms of a polymeric material. Most organic resists contain long chain polymers which either cross link (negative tone resist) or undergo chain scission (positive tone) after irradiation. The polymer chains tend to 'ball up' and form a structure a few nanometers in diameter. Thus the resist has an inherent 'granularity' which influences the minimum feature size possible. In principle this can be circumvented by using an amorphous material such as an inorganic fluoride or oxide[9] as a resist material. Indeed, the 'smallest' individual structures fabricated with high energy electrons have been made using such inorganic materials as resists. However, these materials have their own drawbacks in terms of extreme insensitivity to applied electron dose, complication of preparation and difficulty of processing. As a result, the vast majority of lithography at the smallest dimensions is performed with high molecular weight polymethylmethacryalate (PMMA). For example, in studies of resolution limits of e-beam lithography on high atomic

number substrates, we at NRL have successfully defined 12 nm lines on 60 nm centers in PMMA on tungsten.[10]

The second resolution limiting process is believed to be due to the inelastic scattering of the incident high energy primary electrons. Low energy secondary electrons are created with trajectories essentially perpendicular to the incident beam and broaden the lateral exposure profile in the resist.[11] However, this broadening is clearly underestimated in our present simulations. There is evidence that the range of these low energy secondary electrons is being underestimated by the physical mechanisms currently incorporated in the Monte Carlo simulation. This is an issue which we are continuing to pursue at NRL.

The issue of secondary electrons can be minimized if the primary electrons are of an energy close to the exposure threshold of the resist (a few eV). A low energy approach to nanolithography is discussed below in Section 2.2.

### 2.1.3 Pattern Distortion (Proximity Effects)

In addition to affecting the resolution in e-beam lithography, electron scattering in the resist and substrate results in energy being deposited in the resist at points many microns remote from the point of impact of the primary electron beam. As a result, the size of a given feature is affected not just by the exposure dose given to that feature but also the exposure dose applied to areas of the sample in the vicinity of the feature. This phenomenon is referred to as 'Proximity Effects'.[12]

Correction of proximity effects is a mathematically ill posed problem because their exact correction requires the application of negative amounts of energy with the e-beam which is, of course, physically impossible. However, proximity effects can be reduced by modifying the applied dose supplied by the e-beam. The dose is adjusted pixel by pixel (or feature by feature) to allow for the extra dose absorbed by a pixel from electrons incident on nearby pixels. As a result, the applied dose in dense parts of a pattern is decreased relative to that applied in sparse areas of the pattern.

Research at NRL has concentrated on efficient algorithms for generating pixel by pixel dose adjustments.[13] The 'blurring' of the incident beam exposure profile can be characterized by a point spread function which is dependent only on the incident beam parameters. Thus the effect of the exposure blurring can be described as a convolution of the applied areal exposure dose, $\boldsymbol{D}$ and the point spread function $\boldsymbol{T}$. Thus the absorbed dose $\boldsymbol{A}$ is given by

$\boldsymbol{A}=\boldsymbol{T}\otimes\boldsymbol{D}$, where $\otimes$ represents the convolution operator.(1)

Ideally $\boldsymbol{A}$ should equal the absorbed dose represented by the desired pattern, $\boldsymbol{O}$. One approach to the calculation of the areal dose $\boldsymbol{D}$ required to generate $\boldsymbol{O}$, would simply be to invert equation (1) using, for example, Fourier transforms[14] or matrix inversion.[15] However, these approaches have three drawbacks. First, the inversion of equation (1) is usually ill-posed and hence will not have a unique solution. Second, when inversion is possible, negative values for the areal dose $\boldsymbol{D}$ are almost always generated. Third, even when methods are used to overcome the first two problems, the pattern files relevant to manufacturing production are so large that the necessary numerical calculations are computationally intractable.

An approach to the solution of the inversion of equation (1) is to treat it as a minimization problem, i.e., the solution for $\boldsymbol{D}$ is generated by minimizing:

$$\left|\boldsymbol{T}\otimes\boldsymbol{D}-\boldsymbol{O}\right|^2$$

This approach avoids the numerical difficulties associated with the inversion of the matrix $\boldsymbol{T}$ but does not avoid the problems of generating negative exposure doses.

The generation of negative dose values can be eliminated by the inclusion of a regularizer in the expression (shown above) to be minimized.[13] The choice of a regularizer should reflect additional knowledge that is available about the solution which is not inherent in the minimization expression. We have based the regularizer on the informational or Shannon[16] entropy which is widely used as a metric of positive real valued distributions. Solving the resulting minimization problem generates an optimum (in the mathematical sense) solution to the correction of proximity effects. We have shown that this method is quantifiably superior to existing methods[17] and is susceptible to computation with methods based on artificial neural networks developed here at NRL.[18]

## 2.2 Low Energy Electron Nanolithography

The advantage of a low voltage approach to e-beam lithography in resist materials is that a more spatially localized energy deposition can be achieved than with a focused high energy beam. As a result, proximity effects are virtually eliminated and enhanced resolution and superior pattern fidelity can be obtained.[19] Proximal probes, such as the scanning tunneling microscope or the atomic force microscope with a conductive tip, are convenient ways to realize such a low energy (<50 eV) electron beam with a diameter less than ten nanometers. Furthermore, the energy of the primary electrons can be set close to the energy required to cause a resist material transformation or surface modification, usually the order of a few eV. In contrast, conventional e-beam lithography is performed at energies over four orders of magnitude higher.

A number of material modification mechanisms with lithographic potential have been identified. They are driven either by the flow of electrons between proximal probe tip and sample, the localized electric field beneath the tip or mechanical contact between tip and sample. Demonstrated

processes include selective oxidation, resist exposure, electric field induced ionization, field induced evaporation, indentation, chemical etching, and precursor decomposition. Several reviews of this topic have been published, including a recent survey of the various mechanisms suited to proximal probe based nanolithography.[20]

The potential for ultra fine line lithography has motivated researchers to attempt to implement these ideas into device fabrication as is discussed in the following papers of this issue. Here, the advantage of low voltage nanolithography in polymeric resist films is described. We have shown that thin (30-80 nm) layers of a negative tone polymeric resist (SAL-601 from the Shipley Corporation) can be exposed with the STM operating in the field emission regime (20-50 eV). Although thin, these resist films are sufficiently robust to mask the underlying substrate in a reactive ion etch. The STM lithography results have been compared to lithography with a 50 kV e-beam tool which has a ~10 nm spot size. The exposure conditions for each tool were optimized, but otherwise the resist films were prepared and processed identically. With the STM, smaller feature sizes and narrower pitch gratings are possible than by exposure with the 50 kV e-beam.[19] In addition, STM lithography has a far greater process latitude, i.e., the sensitivity of feature size to incident dose is far less than with the 50 kV electrons.[21]

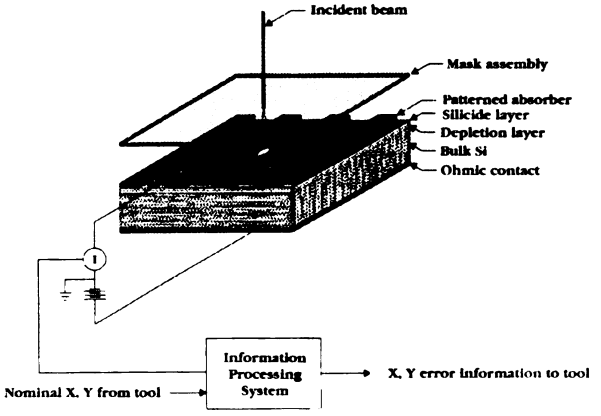
Although only weakly dependent on exposure dose or tip-sample current, feature sizes are proportional to STM tip-sample voltage. Thus varying tip-sample voltage gives a convenient control over feature size. Recently we have been studying the electron optics of the tip-sample region with a view to obtaining a greater understanding of the degree of control required for a reliable and reproducible proximal probe based lithography system.[22] Minimum feature sizes (~20 nm) are obtained at the lowest voltage at which the tip remains just above the resist film which, for a 50 nm film of SAL-601, was measured to be -15 V. To achieve still smaller dimensions, a thinner resist film is required. This has led us to investigate self assembling materials as monomolecular imaging layers for STM lithography as is described in more detail in the following paper by Eric Snow et al..

## 2.3 Feature Placement

As mentioned above, feature placement is becoming the performance limiting issue in e-beam lithography, even at 250 nm design rules where 30 nm feature placement precision is needed. In current practice, the workpiece is mounted on a precision stage which is moved under interferometric control. The distortions of the e-beam deflection system are corrected by scanning precise calibration grids. The actual lithographic writing is performed by a process of dead reckoning assuming that the distortion calibration and stage positioning are exact. In practice this is not the case. Drift of the e-beam due to charging, inaccuracies in the correction of deflection distortions, turbulence in the interferometric path and distortions of the interferometer mirrors are just some of the issues that limit placement precision. Recently, Professor Henry Smith at MIT suggested that the workpiece itself incorporate a fiducial pattern so the position of the e-beam relative to the workpiece can be measured while the lithographic writing is actually taking place.[24] It appears inevitable that such a system is going to be required to improve pattern placement in e-beam nanolithography. The challenge is to find a realizable implementation of this concept, and research to that end continues at MIT and in our group at NRL.[25]

We have concentrated on the problem of pattern placement during e-beam lithography of membrane masks of the type currently envisioned for proximity x-ray and projection e-beam lithographies. During patterning, the majority of the electrons are transmitted through the membrane. So the position of the electron beam incident on the membrane can be measured with an electron detector placed immediately behind the membrane. As a detector, we have designed a reverse biased Schottky diode incorporating a fiducial grid in the form of a patterned absorber on the diode surface. A reverse bias current is induced by the energy deposited by the incident electron beam. This energy (and hence diode current) is reduced where the electron beam first passes through the absorber on the diode surface. Thus the diode current is modulated when the beam is scanned over the membrane/detector assembly. Using Fourier transform techniques one can then interpolate the position of the beam within the period of the patterned absorber layer. The set-up is illustrated schematically in figure 7 (courtesy of F.K. Perkins, NRL).

**Figure 7**
*Schematic of the 'through the mask' approach to in situ beam position measurement for lithography on membrane masks. The membrane mask assembly is mounted on a support ring (not shown). The electron detector (the reverse biased silicon diode) is also attached to the support ring in close proximity to the back of the membrane. The patterned absorber on the surface of the diode enables a measurement of the position at which the incident beam strikes the mask assembly.*



We are currently developing this technique in collaboration with colleagues at the Microelectronics Mask Development project[26] based at IBM's plant in Burlington VT.

The need to measure feature position *in situ* during lithography points to another advantage of proximal probe based systems. Atomic and molecular resolution imaging is relatively commonplace with the scanning tunneling microscope and atomic force microscope. By appropriate control of the probe operating conditions, almost all of the lithographic mechanisms mentioned above can be 'turned off' to allow non-invasive microscopy of the surface of the workpiece. Thus the atomic structure of the surface could be used as a fiducial metric to measure tip position. Admittedly, this would place severe constraints on the preparation of the workpiece and the stability of its surface. These could be alleviated by the incorporation of an ordered monomolecular imaging layer on the surface of the workpiece using a technique such as self-assembly.

Proximal probe instrumentation for lithography is less mature than instrumentation based on high energy e-beams. However, rapid progress is being made and is highlighted in the paper by Professor Quate's group. They report tremendous progress in overcome the inherent slowness of the proximal probes through the batch processing of probe arrays which are optimized for lithographic speed. Non-linearity of the scanners is another problem endemic to proximal probes. Creep, non-linearity and hysteresis lead to large scale pattern distortions for scans much over 100 nm in size. This can be improved by careful electronic design (e.g., charge as opposed to voltage drive) and scanner design (e.g., choice of piezoelectric material) but remains a significant problem for the large (>>1 μm) deflections that will be required for a viable lithographic system. An alternate approach is to move the stage (or tip) under servo control using a position sensor. The Office of Naval Research is currently pursuing an small business innovative research program to build such an instrument. The new system is planned to be more compact, less expensive and less susceptible to atmospheric turbulence than laser interferometer positioning systems. The program is briefly described in the accompanying Research Notes.

# 3. Summary

Our ability to fashion nanostructures from a variety of materials has reached a point of sophistication where it is not just a question of the feature size that can be achieved. Rather, the key challenges lie in the reproducible fabrication of a number of structures with a controlled dimensional range and placement precision. Allowable tolerances for feature size variation and positioning accuracy are typically much less (<20%) than the required feature size. Lithography, the definition of an arbitrary pattern in a sample or sacrificial material applied to the sample surface, is critical to determining the size and placement of a nanostructure. The technique of choice for nanolithography is high energy electron beam lithography because of its well developed equipment base. Precise control of feature size requires a realistic process latitude, i.e., the feature size must not vary excessively with small variations in process parameters such as exposure dose or resist processing times. The problems of spurious beam deflection and position measurement are such that an *in situ* measure of beam positioning will be required for reproducible nanolithography.

A low energy approach to nanolithography using proximal probe based instrumentation has significant advantages in terms of process latitude and feature placement over the more 'conventional' high energy charged particle approach. Advances in instrumentation and processing with proximal probes are occurring rapidly and hold out a realistic hope for the development of a viable nanolithographic technology.

# Acknowledgments

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# Biography

Christie R.K. Marrian is the head of the Nanoelectronics Processing Facility at the Naval Research Laboratory in Washington DC. His current research interests include nanolithography, nanofabrication and the properties of nanometer scale structures and devices.

He obtained his B.A. and Ph. D. Degrees from the Electrical Engineering Department of Cambridge University in 1973 and 1978 respectively. He then spent three years as a post doctoral fellow at the European High Energy Physics Center (CERN) in Geneva, Switzerland. In 1980, he joined the Surface Physics Branch at NRL and initiated a program on Nanoelectronics in 1985 before taking up his present position at NRL in 1993.

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26. This project is sponsored by the DARPA Advanced Lithography Program

# Profiles in Science

## Karl Hess

Professor Karl Hess holds the Swanlund Chair of Electrical and Computer Engineering at the University of Illinois, Urbana, and is Research Professor at the Beckman Institute at the University. For many years, he has been a principal investigator of the Office of Naval Research. Working in areas where science and engineering merge, he is a world leader in the field of hot electrons in semiconductors and computational electronics and often has expanded physical concepts to achieve engineering applications.

Professor Hess developed the concept, theory, and verification of the Real Space Transfer Effect. This effect is basic to high field transport in layered semiconductor materials and transistors. He was the first to develop the theory of the enhancement of impact ionization in photodiodes including layers of superlattices.

Working in the field of metal oxide semiconductor devices, Hess co discovered a significant reduction of hot electron damage by using Deuterium Processing. This work has far reaching consequences for device reliability and proves the role of hydrogen in hot electron degradation.

In the area of computational electronics, he developed the Full Band Monte Carlo method. This numerical simulation technique is now part of computer aided design software, permitting computation of hot electron phenomena (such as impact ionization) with unprecedented precision and scope.

# Nanofabrication with Proximal Probes

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In this paper we describe the use of proximal probes such as the atomic force microscope (AFM) and the scanning tunneling microscope (STM) as a nanofabrication tool. We have developed a resistless proximal probe-based lithographic technique that uses the local electric field of an STM or conductive AFM tip which is operated in air to selectively oxidize regions of a sample surface. The resulting oxide, typically 1 to 10 nm thick, can be used either as a mask for selective etching or to directly modify device properties by patterning insulating oxides on thin conducting layers. In addition to this oxidation process we have also used the STM/AFM to modify the chemical functionality of self-assembling monolayer films. Such modified films are used as templates for the selective electroless plating of metal films. Both of the above processes are fast, simple to perform, and well suited for device fabrication. We have applied the anodic oxidation process to the fabrication of both semiconductor and metal-oxide devices. In these latter structures sub-10 nm-sized device features are easily achieved, and we describe the fabrication of the smallest possible device, a single atomic-sized metallic point contact by using *in situ*-controlled AFM oxidation.

## Introduction

Proximal probes such as the scanning tunneling microscope (STM) and the atomic force microscope (AFM), originally developed to image surfaces with atomic resolution, have recently been used to modify surfaces at the nanometer scale, and have even achieved the manipulation and positioning of single atoms on a surface. This suggests that proximal probes may exceed the limits of electron-beam lithography and perhaps achieve the ultimate goal of atom-by-atom control of material surface modification. This potential has motivated researchers to attempt to implement this level of control into actual device fabrication. However, this task has not been easy due to the irreproducibility of the

modifications, the slow "write" speed and the difficulty of transferring such fine modifications into a functioning semiconductor or metallic device. The challenge has been to overcome these limitations and achieve a reliable process for device fabrication.

At the Naval Research Laboratory we have developed a number of proximal probe-based lithographic techniques that are well suited for device fabrication, and such techniques are now capable of fabricating unique nanometer-scale devices that are difficult to fabricate by any conventional means. These AFM/STM lithographic processes can be used for a variety of applications such as fabricating masks for selective etching [1,2], patterning growth templates by using self-assembling monolayer films (SAMs) [3], and directly patterning the conduction path through thin conducting films [4,5]. In all such applications the fine resolution and high precision imaging properties of proximal probes can be utilized to achieve a unique lithographic tool that is well suited for device fabrication [6-9]. In addition, recent advances in micro-electromechanical device manufacturing make possible the fabrication of large parallel arrays of AFMs. Such advances, when combined with the various AFM lithography techniques, have the potential for high-throughput nanofabrication. These unique features, whether utilized by the bench scientist for prototyping individual devices or potentially by a fabrication facility for high throughput nanolithography, make the AFM a valuable new tool for nanostructure fabrication.

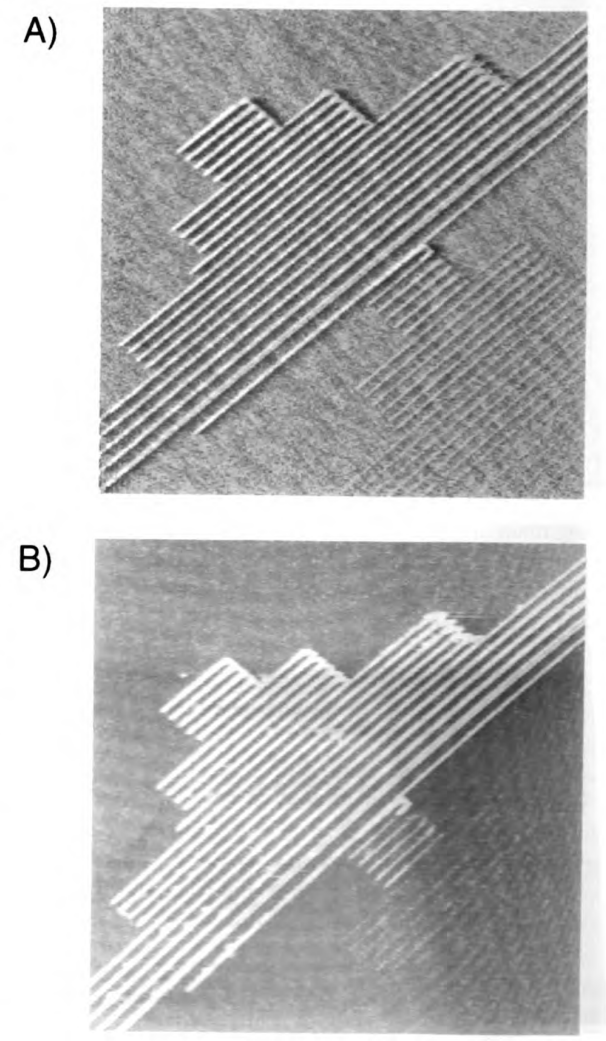
# Proximal Probe Nanolithography

## Oxidation and Selective Etching: Resistless Nanolithography

The application of STM/AFM surface modifications to device fabrication has proven difficult, in part because such probes perform best when modifying very thin layers of material which for the most part are not sufficiently robust for pattern transfer into a semiconductor or metallic structure. Such thin layers are necessary in order to attain fine resolution with probe tips that act as a diverging source of charge or electric field. This restriction does not apply to conventional electron-beam lithography systems that can achieve fine lateral resolution by exposing relatively thick resists with a focused beam of high energy electrons. The key to practical proximal probe-based nanofabrication has been the development of fast, reliable exposure processes that produces a local surface chemical modification that can be used for pattern transfer by using chemically selective processes such as etching. Because such exposure processes modify only the top few monolayers of material and because extremely selective chemical processes are available, both high resolution and effective pattern transfer can be achieved with this approach.

In the most widely employed process, an electrically conducting AFM (or STM) tip that is operated in air is biased with negative polarity relative to a sample and is used to anodically oxidize selected regions of the surface [10, 1]. This process is analogous to conventional electrochemical anodization; however, in this case the cathode of the electrochemical cell is replaced by an AFM/STM tip, and water

**Figure 1**
*5 μm x 5 μm AFM image of a 120 nm pitch oxide pattern written by the AFM (a) and the same pattern as above after etching 10 nm into the surrounding Si (b). The top half of the pattern was written at 2.5 V, the bottom portion at 1.5 V. The shortest lines were written at 1 μm/s while the longest were written at 10 μm/s.*



from the ambient humidity serves as the electrolyte. Under such bias conditions the sample surface is locally oxidized over a lateral range of 10 to 100 nm and to a depth of 1 to 10 nm, the dimensions depending on the type of sample, the shape of the tip, and the exposure conditions. The main advantage of this process is that it provides a simple, reliable process for making a highly local chemical modification to a surface. In addition, the oxidation process is fairly general and can be applied to most materials that can be anodized. The successful application of this oxidation process depends on finding uses for such thin oxides. One application we have explored is the use of these surface oxides as a mask for pattern transfer by selectively etching Si [2].

For the oxidation and etching of Si the sample is prepared by chemically cleaning n- or p-type (100) Si wafers followed by a one minute dip in a 10% aqueous HF solution. The HF solution removes the native surface oxide and passivates the surface with a monolayer of H. This H-passivated surface is stable against oxidation in air. The Si surface is then selectively anodized with the AFM/STM tip to produce surface oxide patterns which are chemically distinct from the H-passivated regions. The oxide patterns are then used a mask for certain selective etches which attack Si but not Si oxide such as KOH or hydrazine.

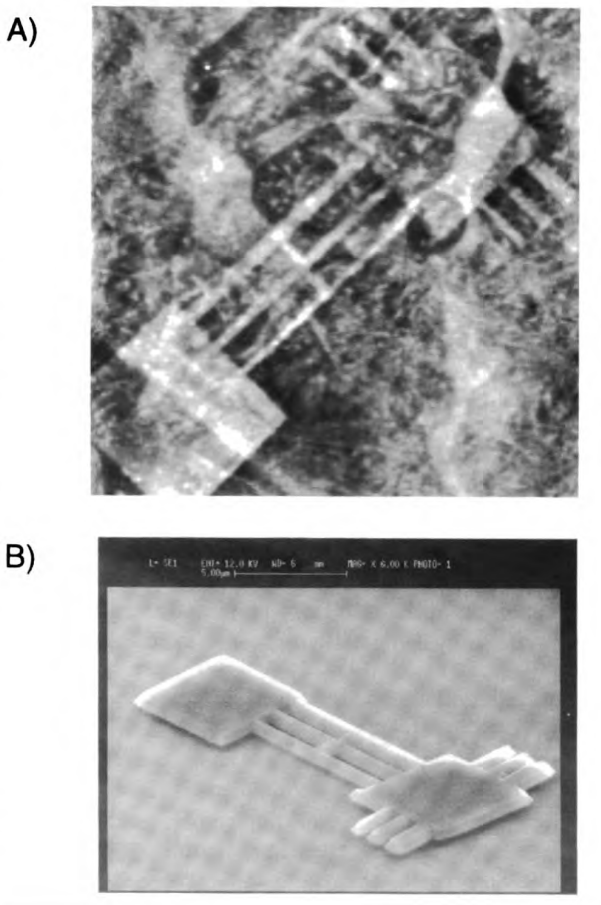
The exposure conditions we use for anodization range from -2 to -10 V tip bias, 0.1 to 100 μm/s write speed and 20 to 60% ambient humidity. The most flexible tool for exposure is the AFM because the exposure mechanism, the tip bias, can be applied independently of the feedback control of the tip-sample positioning. This decoupling of the feedback control allows imaging of the surface without risk of exposure and also allows the AFM to operate on insulating as well as conducting surfaces.

Fig. 1a shows an AFM image of an oxide pattern written by a Ti-coated AFM tip [1]. The AFM image was obtained immediately after writing by using the same tip that wrote the pattern. The act of imaging does not expose the passivated regions of the surface nor does it damage the exposed oxide patterns. The height of the oxide is about 1.5 nm and the period of the grating is 120 nm. The bottom section of the pattern was written at 1.5 V while the top section was written at 2.5 V. All lines were written at the same scanning frequency, so that the longer lines correspond to a higher write speed. The shortest lines were written at 1 μm/s while the longest lines were written at 10 μm/s.

Fig. 1b shows an AFM image of the same pattern after etching 10 nm into the surrounding Si with an 11 Molar aqueous KOH solution [1]. The pattern is faithfully transferred by the selective etch except in the under-exposed regions that were written at 1.5 V. Note in Fig. 1a that the oxide pattern is easily observable and is much more pronounced than the background roughness of the surface. This latent image allows the success or failure of an exposure to be determined prior to etching. For example, the pattern written at 1.5 V was marginally exposed while the pattern written at 2.5 V produced smooth continuous lines. Thus, AFM inspection of the oxide pattern can accurately predict those portions of the pattern that will withstand the etch. The apparent roughness observed on some of the etched lines is not etch irregularities but debris left behind by the etch solution.

For deep etches hydrazine is preferred because of its excellent selectivity against oxidized Si. Fig. 2a shows an AFM image of an oxide pattern written on the surface of a sample of SIMOX [11], a type of Si-on-insulator material that consists of a (100) Si wafer that has been ion implanted with oxygen and annealed to form an electronic grade $SiO_2$ layer buried beneath a crystalline Si surface. In this sample the AFM-generated oxide pattern is difficult to see because of similar dimension features present on the unpatterned SIMOX surface. This oxide pattern, that is ~ 2 nm thick, was transferred into the top Si layer of the sample by a 0.3 μm-deep etch with 70°C hydrazine. The unpatterned Si re-

**Figure 2**
*20 μm x 20 μm AFM image of an oxide pattern written by an AFM on the surface of a sample of SIMOX (a) and a SEM image of the same pattern after it has been etched down to the buried oxide layer with warm hydrazine and partially undercut by etching the $SiO_2$ layer with an HF solution.*



gions were etched down to the buried oxide layer which acts as an etch stop. The buried oxide layer was then etched in an HF solution for a time sufficient to completely undercut the wires and cantilevers but not enough to undercut the square support pads. This step produces the free-standing wires and cantilevers observed in the SEM image of Fig. 2b [11]. Both the uniformity of the etched features and the lack of any pin holes demonstrate the excellent properties of this thin, AFM-generated oxide as an etch mask.

## Silicon as a Resist

While the passivation, oxidation, and selective etching processes are well suited for patterning Si, most other material systems lack the unique surface properties of Si, and a more general lithographic process is required. A general approach to patterning materials other than Si is to cap such materials with a thin Si layer that can be patterned via the above approach and used as an etch mask to pattern the underlying material of interest. In this case, the desired surface properties are achieved by the Si capping layer which can be patterned via the passivation, oxidation, and selective etching process.

As a first test of this approach we used molecular beam epitaxy (MBE) to deposit a thin (~ 5 nm thick) pseudomorphic layer of Si on wafer of GaAs [12]. We used MBE growth in order to achieve a capping layer with surface and etch properties which closely approximate those of bulk Si. Indeed, we have found that such layers are easily patterned with the passivation, oxidation, and selective etching process and that they form an effective mask for etching GaAs. This result represents a first step toward a more general resist-based approach to proximal probe nanofabrication.

Further improvements in this process have been made by eliminating the MBE growth by using hydrogenated amorphous Si (a-Si:H) as the resist layer which can be deposited on a wide range of materials. Examples of this approach include the work of Kramer *et al.* [13], who used HF-passivated and STM-oxidized a-Si:H as a resist layer to etch fine metal wires, and the work of Minne *et al.* [14], who successfully patterned a variety of structures (including a 0.1μ>m gate MOSFET) by using reactive ion etching to selectively etch an AFM-patterned a-Si:H resist layer. This work effectively demonstrates the general application of the anodic oxidation and selective etching process to a variety of material systems by using easily deposited a-Si:H films as a resist layer.

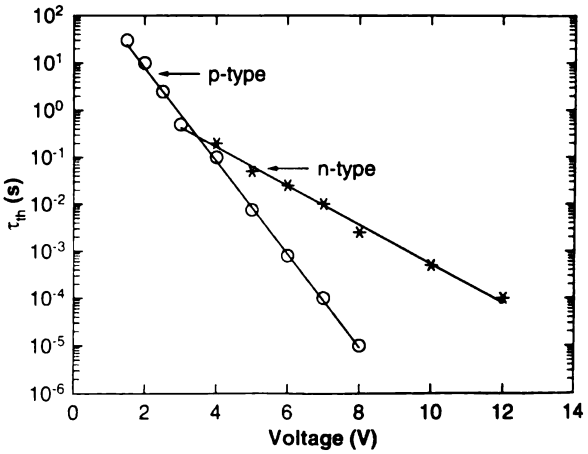
## Limiting write speed

Important issues for any lithographic technique are the ultimate write speed and spatial resolution. This is particularly the case for proximal probe-based lithography which is traditionally very slow. The typical write speeds that we use for AFM oxidation are of order 1 to 10 μm/s. However, it is possible to write at significantly higher speeds, although under such conditions we observe an increased rate of tip degradation. To estimate a maximum write speed for Si anodization, $v_{max}$, we have used voltage pulsing to determine the minimum time required for oxidation, $\tau_{th}$ (i.e. the time required to produce a 1 nm-thick oxide feature), of a (100) Si surface as a function of the magnitude of the voltage pulse, V, applied to Ti-coated AFM tip [1]. $v_{max}$ is then estimated to be $s/\tau_{th}$ where s is the resulting oxide feature size. Over the range of 1 to 10 V we find an exponential dependence $\tau_{th}$ on the applied voltage (see Fig. 3), i.e. $\tau_{th} = \tau_0 \exp(-V/V_0)$ where $\tau_0$ ranges from 1 to $10^3$ s and $V_0$ ranges from 0.25 to 1 V, the exact values depending on the ambient conditions and the tip condition. Consequently, $v_{max} = (s/\tau_0) \exp(V/V_0)$, where s is ~ 30 nm. In principle, $v_{max}$ can be extended to arbitrarily high values by increasing the tip voltage; however, in practice above a limiting voltage the pulse causes damage to the Si surface. This establishes a maximum write speed of ~ 1 mm/s for the oxidation of (100) Si. This observed exponential behavior is consistent with the model of Kramer [15] who suggests that the initial oxidation rate is determined by the desorption of $OH^-$ from the tip and that the desorption rate depends exponentially on voltage.

## Minimum Feature Size

Due to the local nature of the tip-surface interaction and the fact that the generated oxide is only a few monolayers thick, one can expect extremely fine lateral resolution in the exposure process. Indeed, using our air-ambient expo-

**Figure 3**
*Plot of the threshold exposure time $\tau_{th}$ versus voltage for an n- and p-type sample.*

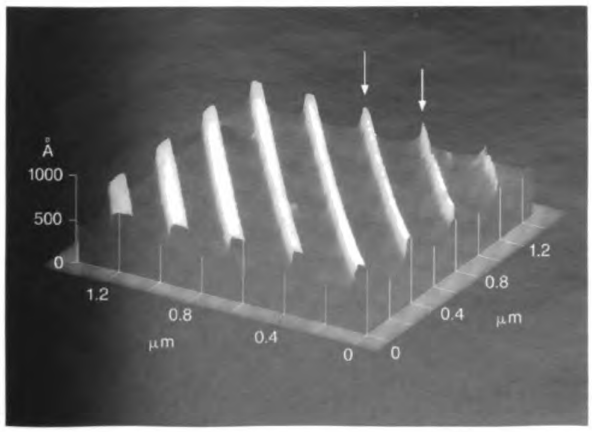


sure process we have produced oxide features with lateral dimensions as small as 10 nm. In addition, Lyding *et al.*, working with an UHV STM can remove the H from a passivated Si surface with near-atomic control [16]. These depassivated regions can then be selectively oxidized by exposure to oxygen [17], although pattern transfer has not yet been demonstrated with these UHV-formed oxides. While this UHV process demonstrates the ultimate potential of the exposure process, continued improvement in the size of etched features requires directional dry etching techniques which can improve the limited aspect ratios obtained by liquid etching.

To explore the resolution limits of etched features we have used an electron cyclotron resonance (ECR) source to etch Si nanostructures that were patterned by selective oxidation of a H-passivated Si surface with an AFM [18]. ECR etching provides both the necessary chemical selectivity and directionality to etch high aspect ratio features masked by the thin, AFM-generated oxide patterns. The patterns were etched in a $Cl_2$ plasma generated by an ECR source. The etch conditions were optimized to provide high selectivity over the oxide mask, a vertical etch profile, and smooth surface morphology. Si nanostructures with ~ 10 nm width and 30 nm depth were etched in a $Cl_2/O_2$ plasma (see Fig. 4). Wider structures with a thicker oxide were etched to a depth of 70 nm with no signs of mask degradation.

This result indicates that ambient AFM-oxidation in combination with selective dry etching is suitable for fabricating structures with lateral dimensions as small as 10 nm. Combining this etching technique with the UHV-based exposure process should be capable of producing structures in the 1 to 10 nm range. Structures of such fine dimensions are not easily attainable with conventional fabrication techniques.

**Figure 4**
*AFM image of a pattern etched into a Si sample by using an $Cl_2$ plasma generated by an ECR source. The etch depth was 30 nm. The two lines indicated by the arrows have linewidths of ~ 20 nm and ~ 10 nm.*




The fact that such small structures are easily fabricated and can be adapted into device fabrication schemes illustrates an important, unique aspect of proximal probe-based nanolithography and indicates that such lithography will be an integral part of future nanostructure science and technology.

## Self-assembled monolayer films

An aspect of proximal probe lithography (PPL) that is often overlooked is the utility of imaging layers. Imaging layers are used in other lithographic technologies as a means of recording a pattern produced either by masking, as with photon-based processes, or by direct writing, as with *e*-beam writers. While several schemes have been demonstrated that record information written by proximal probes, these schemes are limited in terms of speed, range of substrate applicability, or sensitivity to various etch processes, to name a few. For this reason we have devoted considerable effort to finding imaging layers suitable for high speed, high resolution lithography based on pattern transfer of STM and AFM generated patterns.

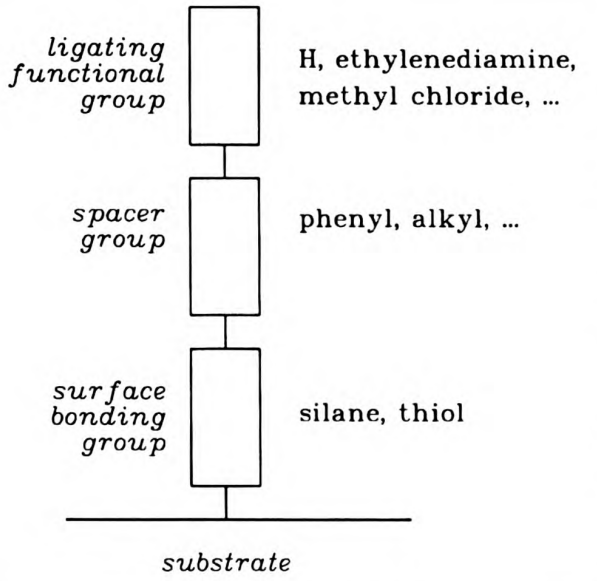
Polymeric films, such as commercial *e*-beam resists poly(methylmethacrylate) and SAL-601-ER7™, have demonstrated high resolution capabilities in STM lithography [19], and investigations are currently underway to investigate their suitability for AFM-based lithography. Unfortunately, films sufficiently thin to be compatible with the current feedback mechanism of an STM are generally too thin to make useful etch masks or defect-free lift-off layers.

Self-assembled monolayer films (SAMs) have not only demonstrated high resolution [20], but also compatibility with PPL [21] and functionality as a hard etch mask [3]. Because the mechanism that drives self-assembly is a highly energetic chemisorption reaction, films based on these materials have an extremely low defect density, are quite environmentally stable, and are mechanically robust. Insofar as it affects PPL, the precursors from which SAMs are grown may be thought of as consisting of three parts, as shown in Fig. 5: a substrate binding part, a spacer part, and a surface functionality part. While these parts are not quite fully interchangeable from one molecule to the next, different considerations are appropriate for the selection of each.

For the surface binding part, a silane ($RSX_3$) is used to bind to hydroxol (OH) groups typically found on Si and Pt. Hydrogen substituents on the silane (the "X" part) are most commonly methoxy groups ($CH_2O$), Cl, or a mixture of the two. The composition of the surface binding part strongly affects both film ordering and the tendency of the film to grow multilayers, and to a lesser extent the packing density. A thiol (RSH) forms highly ordered layers on surfaces of GaAs or Au.

The spacer part has an effect on the interaction of the film with the patterning tool. By moving the functional part

**Figure 5**
*Component representation of precursor molecules used for self-assembled monolayer film growth.*



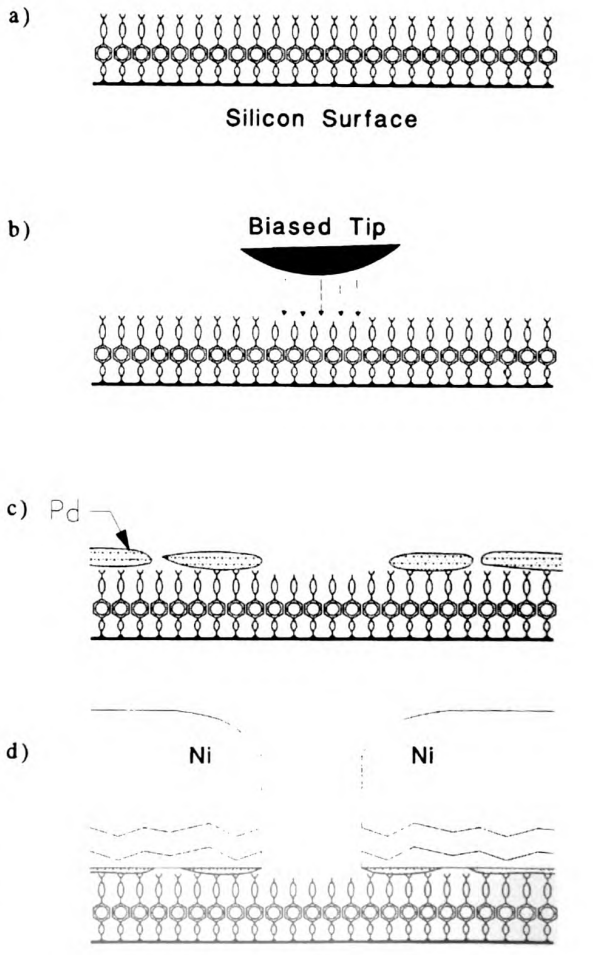

away from the surface and closer to the high field of the tip, long spacer groups (multiple $CH_2$ groups, for example) can lower the dose or voltage threshold for exposure [21]. The conjugated bonds found in phenyl groups are also somewhat conductive, and hence more amenable to STM operation.

The surface functional group actually defines the "new" surface. For example, amine ($NH_2$) groups can be used as ligation sites for certain molecules. While not particularly active themselves, halides (Cl, I, *etc.*) have an extremely high cross-section for electron capture and subsequent desorption of the halide fragment. Subsequent processing can be based either on replacing the halide atom with a more reactive functional group, or on acting upon the fragment remaining after halide desorption. Alkyl terminated surfaces are extremely inert and hydrophobic, being chemically identical to paraffin. As such, they have been used for pattern transfer as masks against wet etching [22], and to a limited extent, dry etching. They have also been used to *enhance* STM-induced etching of gold.

Most investigations of functionalized monolayers as imaging layers for PPL have used organosilanes to grow films on Si. We have used a Pd-containing oligimeric colloid as an intermediate step in the eventual generation of a high resolution patterned Ni layer, also useful as a hard etch mask [22]. This process is illustrated in Fig. 6. After cleaning and hydrogen passivation in dilute HF, the wafer sample is immersed briefly in a solution of the monomer, removed, and dried on a hot plate. The resulting film thickness is on the order of 1 to 1.3 nm. After STM patterning (and ligand grafting, in the case of certain films) the sample is immersed in the colloidal Pd, which selectively ligates onto the unexposed film forming a layer 2.6 nm thick. The sample is subsequently rinsed and again immersed in a nickel borate electroless plating bath, where nucleation of the Ni is catalyzed by the Pd. In this way, we have been able to write gaps between Ni pads as small as 15 nm, and then transfer them through reactive ion etching into Si (Fig. 7). The Ni growth is somewhat anisotropic and tends to smooth rough edges. The rms roughness of the pattern edges is generally below 3 nm. The Ni may be easily removed after patterning by immersion in the catalyst solution.

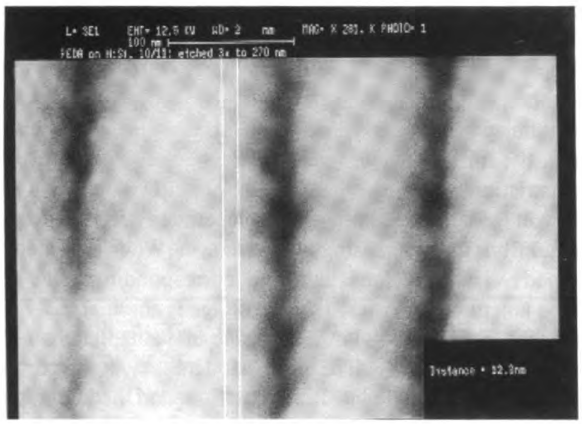
We have investigated exposure characteristics of several organosilane films using a vacuum STM:

**Figure 6**
*Schematic illustrating replication of a high resolution pattern in a STM exposed SAM film. Starting SAM film (a); pattern generation by using a STM as a source of low-energy electrons to interact with and expose the film (b); ligation of Pd catalyst (c); electroless growth of Ni from solution (d).*



octadecyltrichlorosilane [OTS], (aminoethylaminomethyl) phenethyltrimeth-oxysilane[PEDA], chloromethylphenyltrimethoxysilane[CMPTS], chloromethylphenethyl-trimethoxysilane [CMPETS], and monochlorodimethoxysilane versions of PEDA and CMPTS.

**Figure 7**
*Narrow trenches etched into Si created by the process illustrated in Fig. 6.*




The threshold exposure voltage is primarily determined by the end group, and is generally reduced about 2 to 3 V for films grown on passivated Si rather than the terminal native oxide. We have also used a conducting tip air ambient AFM to modify a PEDA film deposited on the native oxide of a Si surface and observed an exposure threshold of 5V [23].

# Device Fabrication

## Device Fabrication by using Selective Oxidation as an Etch Mask

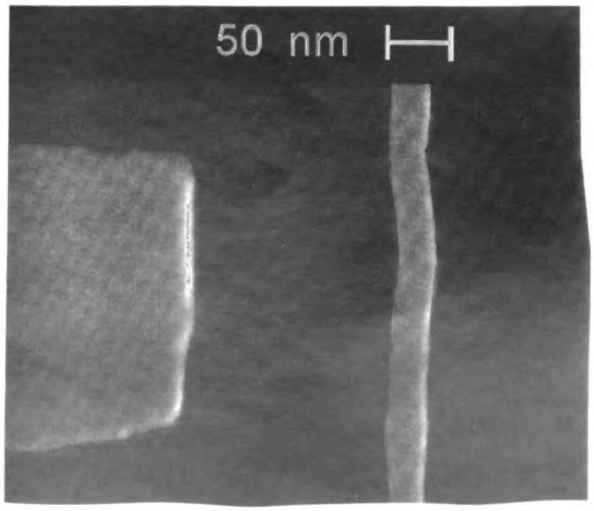
A unique feature of AFM-based lithography is the fact that the exposure and imaging mechanisms of the AFM operate independently. Thus, high resolution images of the sample can be obtained and used for precise pattern alignment without risk of exposure. In addition, latent imaging of an exposed pattern allows the success of an exposure to be assessed and corrected before further processing. Combining these imaging capabilities with the high resolution exposure process make the AFM a unique lithographic tool well suited for fabricating critical features in nanometer-scale devices. As a demonstration of this capability we have used AFM-defined oxide patterns and selective etching to fabricate side-gated Si field-effect transistors with critical dimensions as small as 30 nm [7].

The devices consist of an etched Si wire between two contact pads and a lateral gate that is isolated from the wire by a small air gap. The wire and gate are isolated from the substrate by using SIMOX. The buried oxide layer of this material forms an effective barrier to isolate the device structure from the substrate. Both the source-drain channels and the side gates were patterned by the AFM while the ohmic contact pads for source, drain and gate were formed by optical lithography.

The devices were fabricated as follows. First optical lithography was used to deposit the metal ohmic contact pads. The samples were then cleaned and H-passivated. The AFM was used to image these pads and to align the tip for exposure of the source-drain channel and the side gate. After exposure the oxide patterns were imaged to check the success of the exposure. If any defects were detected the pattern was corrected before further processing. After the exposure was completed a sample was then etched in 70° C hydrazine to remove all of the surface Si layer that was unprotected by the oxide pattern or the metal pads down to the buried oxide layer that acts as an etch stop. Fig. 8 is a SEM image of a completed device that is fabricated on a top Si layer that is 40 nm thick. The source-drain wire shown in the figure is ~ 30 nm wide by 40 nm high by 6 μm long. The lateral gate finger can also be seen.

While the device shown in Fig. 8 serves as a functioning field-effect transistor [13], this basic structure can also be used as a building block for fabricating quantum-effect devices. For example, the source-drain channel could be modified to contain a small island. A sufficiently small is-

**Figure 8**
*SEM image of the active region of a side-gated transistor fabricated from SIMOX. The width of the source-drain channel is ~ 30 nm.*



land would generate quantum effects arising from discrete quantum levels in the island. It should also manifest single electron charging effects (also known as the Coulomb blockade) that occur when the island capacitance C is small enough that a single electron transferring onto the island creates an electrostatic charging energy $E = e^2/2C$ which blocks a second electron from transferring to the island. Both of these effects depend on fabricating sufficiently small structures such that the quantum confinement energy or the charging energy is greater than kT. Several groups report the use of electron beam lithography to fabricate such structures from SIMOX [24 - 26]. In all cases thermal oxidation is used to shrink the size of the structures following etching such that quantum or charging effects are observable well above 4 K. Proximal probe lithography may provide a means to fabricate structures with dimensions small enough to manifest these quantum and single-electron charging effects at room temperature, which would open the way for their use in practical applications.

## Selective Oxidation for Direct Device Modification

An alternate approach to the two-step technique described above (oxide pattern definition followed by pattern transfer by etching) is to use the AFM-generated surface modifications to define device properties directly. Such an approach has the advantage that the electrical properties of a device can be monitored in real time and tuned to specifications by the anodization. In addition, because the geometry of a device is related to its electrical properties, sub-10 nm feature sizes are easily achieved by using such real-time measurements as a guide for the fabrication.

In particular, we have used selective oxidation of thin metal films to define narrow metal wires by oxidizing the unwanted regions of wide metal wires [5]. We have also used this process to fabricate lateral metal-oxide-metal tunnel junctions by introducing thin regions of oxide in an otherwise continuous metal film [4, 5]. Such lateral metal-oxide-metal junctions can be made very small and, thus, have correspondingly small junction capacitance. These narrow wires and tunnel junctions form the building blocks from which more complex quantum devices can be built. Recent examples of such quantum devices include a single-electron transistor (SET) by Matsumoto et al. [8] and a single-atom-sized metallic point contact by us [9], both of which exhibit room temperature quantum effects because of the small sized achieved by using proximal probe-based anodization.

In our work described in Ref. [5] and [9], the point contacts and tunnel junctions were formed by using the AFM to anodize through the cross section of Al or Ti nanometer-scale wires while using *in situ* electrical measurements as feedback to guide the anodization. These metal wires were formed by first using optical lithography and metal liftoff to pattern ~ 1 μm-wide by 5 to 8 nm-thick metal wires, each connected to contact pads. The nanometer-scale patterning of these structures was accomplished by using selective anodization with the AFM.

A diagram of the fabrication circuit is shown in Fig. 9. The AFM is first used to define a small constriction (typically 40 nm-wide by 500 nm-long, but ones as narrow as 5 nm have been made) in the middle of a 1 μm-wide metal wire [5]. This is done by oxidizing the outer portions of the wire, leaving only the center metallic. In order to achieve the level of control necessary for this step, the electrical resistance of the wire is monitored during the oxidation process. When a resistance corresponding to the desired width is obtained, the tip bias is automatically set to zero, thus terminating the oxidation process. To form a lateral oxide junction, the tip is scanned repeatedly across a section of this constriction while slowly increasing the tip voltage. As the tip voltage is increased the oxide penetrates deeper into the metal film, thus increasing its resistance. When a predetermined resistance value is achieved, corresponding to the desired junction properties, the tip voltage is automatically set to zero. Fig. 10 shows an AFM image of a completed single oxide junction device. The 1 μm-wide metal wire, the oxide that defines the 40 nm-wide constriction, and the lateral oxide barrier (highlighted by the circle) are visible.

If the oxidation procedure is continued until the oxide penetrates almost completely through the metal wire, most parallel conduction paths will be shut off. As the size of the remaining metal conduction channel decreases it eventually approaches the limit of ballistic conduction through a one-dimensional channel, for which the conductance becomes quantized in units of $2e^2/h$. In order to achieve this regime of quantized conductance the current flow must be constricted to a region of size $\sim\lambda_f/2$, where $\lambda_f$ is the Fermi wavelength.

**Figure 9**
*Diagram of the circuit used for fabricating the metal/oxide device structures. The device current was measured in real time during the fabrication to guide the anodization.*

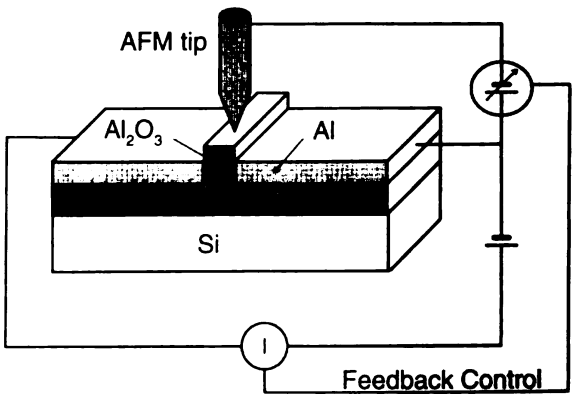
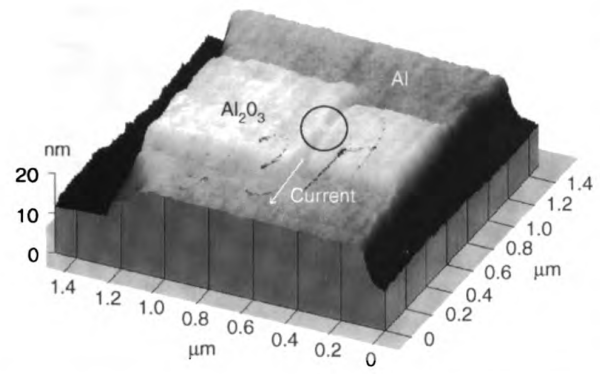


**Figure 10**
*AFM image of an Al/$Al_2O_3$ lateral metal/oxide/metal junction. The current is first constricted down to a ~ 40 nm-wide wire and passes through the lateral metal/oxide junction indicated by the circle. The oxide features are the raised, lighter areas.*



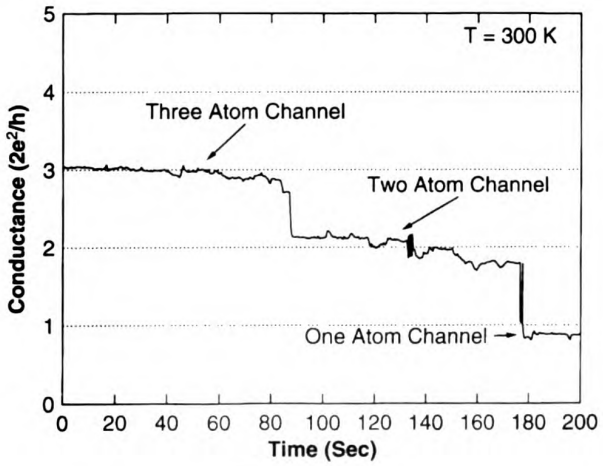

For metals, because $\lambda_f/2$ is ~ 0.2 nm, a quantized conductance of $2e^2/h$ indicates a conduction channel the size of a single atom. These atomic sized conduction channels form the point contacts, and they are evidenced by the discrete decreases in conductance ~ $2e^2/h$ (shown in Fig. 11) as these last remaining atomic channels are closed.

Fig. 11 plots the time dependence of the conductance of an Al point-contact device after the tip voltage was set to zero, and indicates that additional oxidation events occurred during this time. These oxidation events correspond to the large discrete steps to lower conductance which close the remaining conduction paths. These steps occurred in approximate but not exact units of $2e^2/h$. This deviation from exact quantization can arise from a number of sources such as electron scattering, the detailed electronic wavefunctions of the Al atoms, and from series resistance of the thinned Al layer leading to the actual atomic-sized point contact. The device eventually stabilized at a conductance value $\cong 2e^2/h$ that corresponds to a single, atomic-sized conductance path. In such stabilized devices, it is possible to maintain a stable one-atom point contact over a period of a day or more. Such atomic-sized wires demonstrate the level of control that is achievable by using real-time electrical measurements as feedback to guide the AFM anodization.

As the last remaining conduction path is closed, the conduction through such devices changes from metallic to tunneling. In Al structures it is difficult to achieve a reproducible tunneling resistance because the large Al/$Al_2O_3$ barrier height ( ~ 2 eV) results in large discrete resistance changes for each subsequent oxidation event. In contrast, by using Ti/$TiO_x$, which has an approximately order of magnitude smaller barrier height, tunnel junctions with predetermined resistances can be made.

Such control of the tunneling resistance, combined with the intrinsically small capacitance of the lateral geometry, make the Ti/$TiO_x$ system attractive for lateral tunnel-junction devices. Matsumoto *et al.* recently reported the fabrication of a room-temperature-operational SET by using STM-anodization of a thin Ti film [8]. In addition, we are exploring a novel nanometer-scale transistor that operates by using a gate to modulate the current passing through such a lateral tunnel barrier. AFM anodization provides a powerful tool for exploring such novel metal/oxide-based quantum devices.

**Figure 11**
*Conductance of an Al/$Al_2O_3$ junction as the last remaining conductance channels are cut off. The conductance is quantized in approximate units of $2e^2/h$. A conductance of $2e^2/h$ corresponds to a one-atom conductance channel.*




# Summary

Over the past few years much progress has been made in the development of proximal probes for use as a nanolithography tool. AFM/STM anodic oxidation combined with selective etching provides a simple, reliable process for fabricating nanostructures and nanometer-scale devices. In addition, this oxidation process combined with *in situ* electrical measurements can be used to directly pattern metal/oxide devices with feature sizes well below 10 nm and in some cases down to atomic dimensions. Such control has opened up the exploration of new classes of devices which are based on lateral metal/oxide tunnel junctions. Another promising approach to proximal probe lithography is the use of self-assembled monolayers. Such films offer the potential for high speed exposure as well as practical functionality such as serving as templates for metal growth. Such high-speed processes combined with parallel arrays of microfabricated proximal probes offer the potential for a unique, high-throughput nanolithography tool.

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# Biographies

Eric S. Snow is a research physicist in the Electronics Science and Technology Division at the Naval Research Laboratory. His current research is in the area of nanostructure science and technology and includes such specialties as proximal probe-based nanofabrication, nanoelectronic devices, and near-field optical studies of quantum dots. He received the Thomas Edison award for his patent for AFM lithography. Dr. Snow obtained his Ph.D. in physics at the University of North Carolina at Chapel Hill in 1986. From 1986 to 1987 he was a National Research Council - Naval Research Laboratory Postdoctoral Associate. He became a permanent member of the NRL research staff in 1987.

Paul M. Campbell received a Ph.D. in physics in 1980 from the Pennsylvania State University. From 1979 to 1985 he was a physicist at the General Electric Corporate Research and Development Center in Schenectady NY, where he performed research in compound semiconductor materials, processes, and devices. In 1985 he became a research physicist in the Electronics Science and Technology Division of the Naval Research Laboratory, where he studied the transport and optical properties of semiconductor heterostructures and nanostructures. He is currently exploring the use of proximal probes for the fabrication of nanostructures.

Keith Perkins received a BS in Physics from the Massachusetts Institute of Technology, and an MS and PhD. in Materials Science from the University of Wisconsin-Madison in 1988 and 1992, respectively. He came to the Naval Research Laboratory on a National Research Council fellowship where he has investigated applications of the scanning tunneling microscope in nanolithography. He has published several papers based on this and other novel nanolithographic technologies.

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# UHV STM Nanofabrication: Progress, Technology Spin-offs, and Challenges

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## Abstract

Scanned probe microscopy (SPM) is emerging as an important new route for nanofabrication in a variety of systems. One SPM nanofabrication method with potential technological relevance for modifying silicon surfaces is the ultrahigh vacuum (UHV) scanning tunneling microscope (STM). This paper reviews the use of the UHV STM for atomic scale nanofabrication on hydrogen passivated silicon surfaces. By simple analogy this can be thought of as the limiting extrapolation of e-beam/resist technology to atomic dimensions. The method reviewed here describes the use of the UHV-STM to selectively desorb hydrogen from silicon with atomic scale precision. The resultant patterned surface then serves as a template, utilizing the chemical contrast between clean and H-passivated silicon, for selective chemistries including oxidation, nitridation, and metallization by thermal chemical vapor deposition (CVD). In conjunction with the nanofabrication, important basic scientific issues such as the fundamental mechanisms for hydrogen desorption are elucidated. It is during these studies that the dramatic deuterium isotope effect was discovered, whereby deuterium is nearly two orders of magnitude more difficult than hydrogen to desorb from silicon. This discovery led to the idea of using deuterium, instead of hydrogen, to passivate the dangling bonds at the oxide/silicon interface in metal oxide semiconductor (MOS) transistors in order to reduce hot-carrier degradation effects. Transistors treated with deuterium show lifetime improvements by factors of 10 to 50.

## I. Introduction

In recent years scanned probe microscopy (SPM) has expanded dramatically from its basic scientific role into areas of current and future technological development. The scanning tunneling microscope (STM) and atomic force microscope (AFM) have led the way by merging atomic resolution characterization with nanofabrication capabilities. This paper focuses on one of the SPM techniques, the ultrahigh vacuum (UHV) STM, in its role as a nanofabrication and

characterization tool. These combined capabilities can be particularly powerful as demonstrated by the recent discovery of the large deuterium isotope effect.[1,2] This discovery helped provide the basis for the use of deuterium processing to dramatically improve the lifetimes of complementary metal oxide semiconductor (CMOS) transistors with regard to hot electron degradation effects.[3]

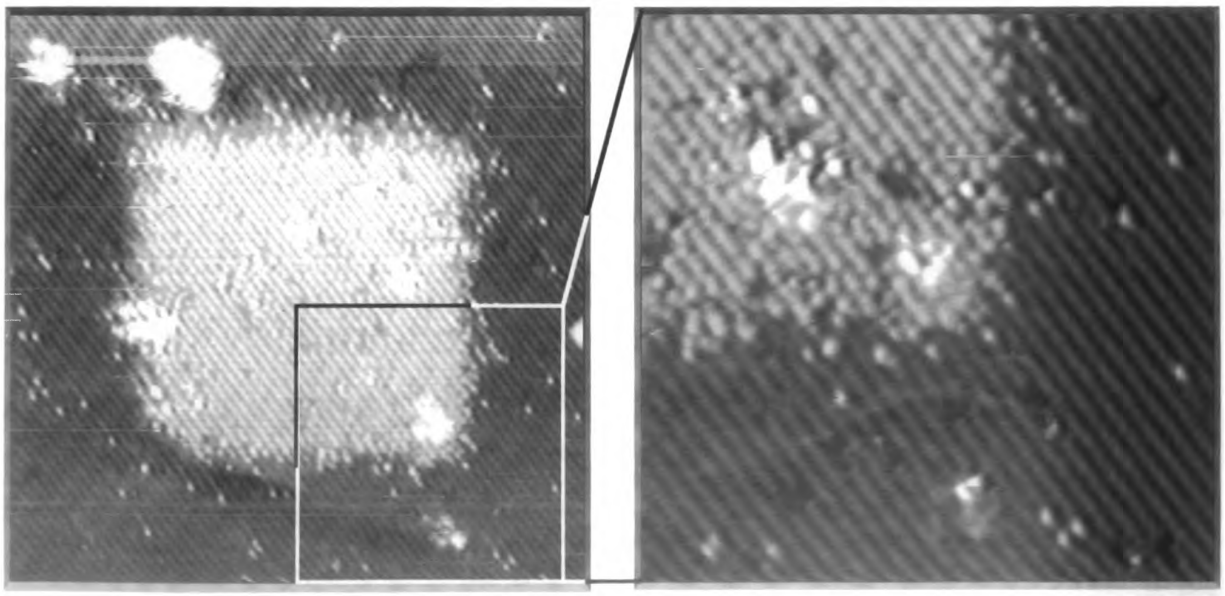
A very intriguing system which has been explored in recent SPM nanofabrication experiments is hydrogen passivated silicon. Dagata and co-workers showed by ambient STM that wet passivated Si(100) surfaces could be patterned by raising the STM tip voltage sufficiently to disrupt the hydrogen passivation layer.[4] By scanning the tip they were then able to write ~100 nm wide lines of thin oxide in any desired pattern. Snow and co-workers extended this technique by using the thin oxides as masks for wet etching[5] and electron cyclotron resonance anisotropic etching[6] to achieve pattern transferred linewidths as narrow as 10 nm. An important extension of this nano-oxidation scheme to hydrogenated amorphous silicon (a-Si:H) was demonstrated by Schönenberger et al.[7] This is significant since a-Si:H can be deposited on a wide variety of substrates. Using a-Si:H layers patterned by a conductive tip AFM, Quate's group fabricated the gate region of a 0.1 μm CMOS transistor exhibiting high performance electrical characteristics.[8] Snow and Campbell have also made gated transistor structures by this technique.[9]

While much progress has been made utilizing ambient SPMs to nano-oxidize silicon, a parallel approach has evolved using the UHV STM to pattern H-passivated silicon. The UHV STM offers the ability to explore fundamental resolution limits, obtain quantitative information about the mechanisms for H desorption, and to explore a variety of selective chemical processes by preserving pristine surface conditions. The first study of hydrogen desorption by UHV STM was by Becker et al for H-passivated Si(111) surfaces prepared by wet chemical methods.[10] Becker's work, combined with Dagata's ambient STM lithography, motivated our development of the UHV STM-based nanolithographic scheme for H-passivated Si(100) surfaces discussed in the next section of this paper.[11]

# II. UHV STM Nanolithography of H-Passivated Silicon

The initial goal of this work was to explore the use of hydrogen as a monolayer resist on Si(100) surfaces.[11] To avoid the contamination associated with wet chemical processing, H-passivated Si(100) samples were prepared under UHV conditions. First, the atomically clean Si(100) surface is pre-

**Figure 1**
*(a) A 500 Å x 500 Å STM image of a H-passivated Si(100) surface where the central 290 Å x 290 Å region has been depassivated by raster scanning with the tip biased at -5.5 V relative to the surface. (b) A 240 Å x 240 Å STM image showing dimer resolution detail of one corner of the patterned area shown in (a).*



(a) (b)

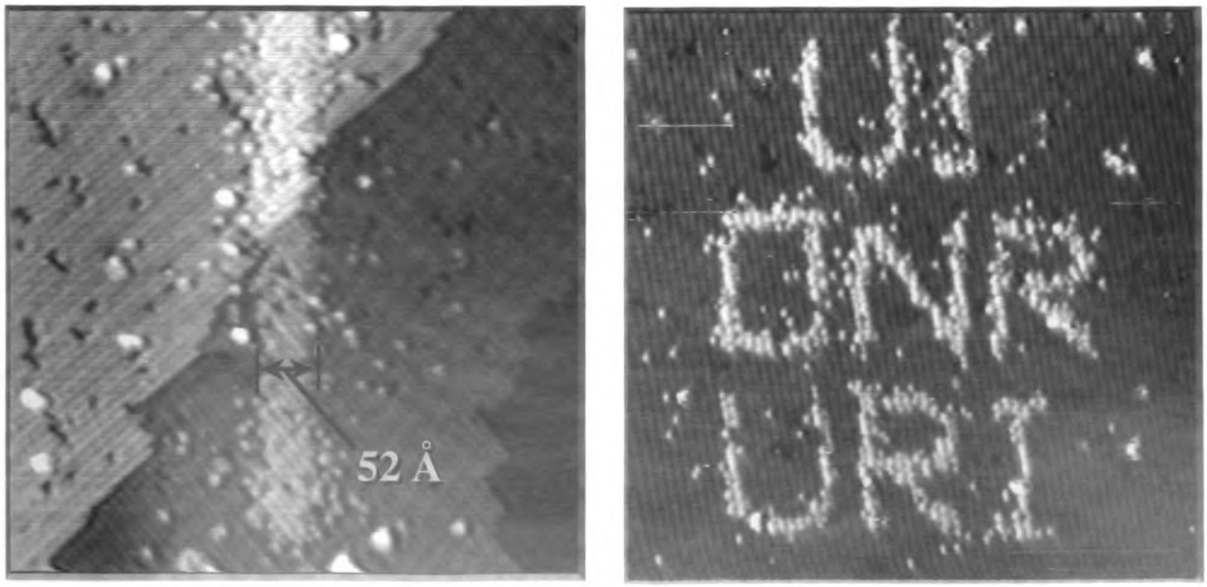
pared by heating the sample to ~1250 ° C for about one minute in the UHV chamber. Next, H-passivation is achieved by exposing the surface to atomic hydrogen obtained by cracking molecular hydrogen with a hot tungsten filament placed near the sample. By heating the silicon sample to ~650 K during this process, etching is avoided and each surface silicon atom becomes terminated by a single hydrogen atom. The UHV STM design used for the work reported here features low thermal drift, and the ability to register the atomic resolution scan window with substrate features over mm dimensions.[12,13]

Under normal scanning conditions the UHV STM does not perturb the H-Si(100) surface. However, hydrogen can be desorbed by increasing the voltage between the STM tip and the sample. This is demonstrated in fig. 1 where hydrogen has been removed by raising the tip voltage to 5.5 V (tip negative) and raster scanning it over the central square region. The clean depassivated silicon appears brighter (1.5 Å higher) due to its increased density of states available for tunneling. The well defined boundaries of the pattern shown in fig. 1 suggest higher resolution capability for single line patterning. This is demonstrated in fig. 2 for patterning at two different voltages, 7 V and 4.5 V. The line patterned at 7V is ~5 nm wide and was written using a current of 0.1 nA and a line dose of $10^{-4}$ C/cm. At 4.5 V the linewidth has decreased to ~1 nm reflecting the transition into the tunneling regime where higher resolution is expected. Aside from enhanced resolution it was determined that patterning at lower voltages requires higher current.[11] The lines in fig. 2b were written at 4.5 V, 2.0 nA, and 2 x $10^{-3}$ C/cm. Patterning at 4.5 V does not occur if lower currents such as 0.1 nA are used. Another important observation is that hydrogen desorption only occurs when the tip is biased negative relative to the sample. In this case, electrons impinge on the surface with maximum kinetic energy. No hydrogen desorption is observed for positive tip biases (up to 10 V).

The STM patterning experiments suggest two regimes for hydrogen desorption; a dose dependent regime at higher voltages and a current and voltage dependent regime at lower voltages. To explore these regimes, experiments were performed to determine the number of electrons needed to desorb hydrogen.[14] Fig. 3 shows plots of the desorption yield (atoms/electron) determined from these experiments. From fig. 3a it is clearly seen that the desorption yield is constant above ~7 V. This is the electron stimulated desorption (ESD) regime in which individual electrons have sufficient kinetic energy to excite the Si-H bonding-to-antibonding transition (see inset). Once in the antibonding potential the hydrogen experiences a repulsive force accelerating it away from the silicon atom. If the residence time in the antibonding state is sufficiently long then the kinetic energy gained, $E_{kin}$, exceeds the escape energy barrier of the bonding potential, $E_{esc}$, and desorption occurs. From the data in fig. 3a it is seen that desorption above 7 V occurs for approximately one in every

**Figure 2**

*(a) A single line patterned with -7 V applied to the tip. The line was written with a current of 0.1 nA and a line dose of 1.0 x $10^{-4}$ C/cm. (b) The letters "UI ONR URI" written with 1 nm wide lines patterned at 4.5 V, 2 nA, and 2.0 x $10^{-3}$ C/cm.*




(a) (b)

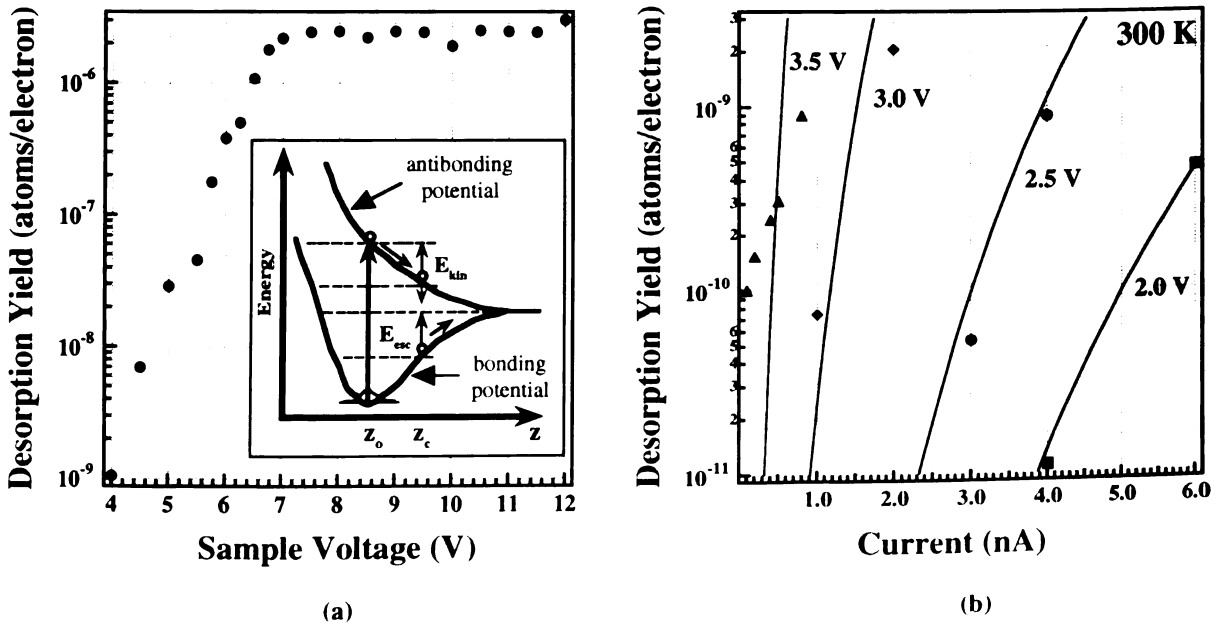
400,000 incident electrons. In this regime H-desorption depends on the electron dose, not on the voltage or patterning current. Below 7 V, however, H-desorption is still observed even though individual electrons no longer have sufficient energy to excite the bonding-to-antibonding transition. The desorption observed in this regime is described well by the vibrational heating model postulated in advance of these experiments by Avouris' group at IBM Watson Research Laboratory.[15] The vibrational heating of the Si-H bond stems from the fact that its vibrational mode has a long excited state lifetime since its high frequency (due to the low hydrogen mass) results in poor coupling to the substrate phonon modes. During tunneling some of the STM electrons excite this vibrational mode via inelastic processes (which depend on voltage); and in fact, at nA current levels it is possible to achieve multiple excitations of the Si-H vibrational system.[15] Consequently, if the excitation rate (which depends on current) exceeds the de-excitation rate (which depends on phonon coupling) then the Si-H mode accumulates energy over time, eventually leading to desorption. Fig. 3b shows the strong current and voltage dependence expected for the vibrational heating regime. As will be seen later in this paper, the detailed understanding of the desorption mechanism has implications that go well beyond basic scientific interest. However, first we will discuss important aspects of nanofabrication associated with the use of STM patterned H-passivated silicon.

# III. Selective Chemistry

Future electronic devices and circuits will depend on the ability to fabricate nanoscale insulating and metallic structures. The ability to pattern H-passivated silicon with nanometer precision is only one step in that direction. Further development of this route towards nanofabrication depends on taking advantage of the strong chemical contrast between H-passivated and clean silicon. We are exploring this issue by performing experiments that include the selective oxidation, nitridation, and metallization of the STM patterned surfaces. Figs. 4a,b show examples of selective oxidation in which the surface is dosed with oxygen in the UHV chamber after STM patterning.[11] This results in the initial oxidation of the exposed clean silicon as evidenced by the mottled appearance in the patterned area after dosing. Similar experiments have also been performed using much higher oxygen doses to achieve thicker oxides.[16] In both cases the hydrogen passivated regions remain unaffected by oxygen dosing. Selective nitridation has been accomplished by treating the STM patterned surface with ammonia ($NH_3$).[17] Fig. 4c shows a STM patterned square region following a 2 L [1 L (Langmuir) = $10^{-6}$ Torr sec] $NH_3$ dose in the UHV chamber. The inset shows the clean silicon pattern prior to the dose. While the $NH_3$ treatment appears to repassivate the surface,

**Figure 3**

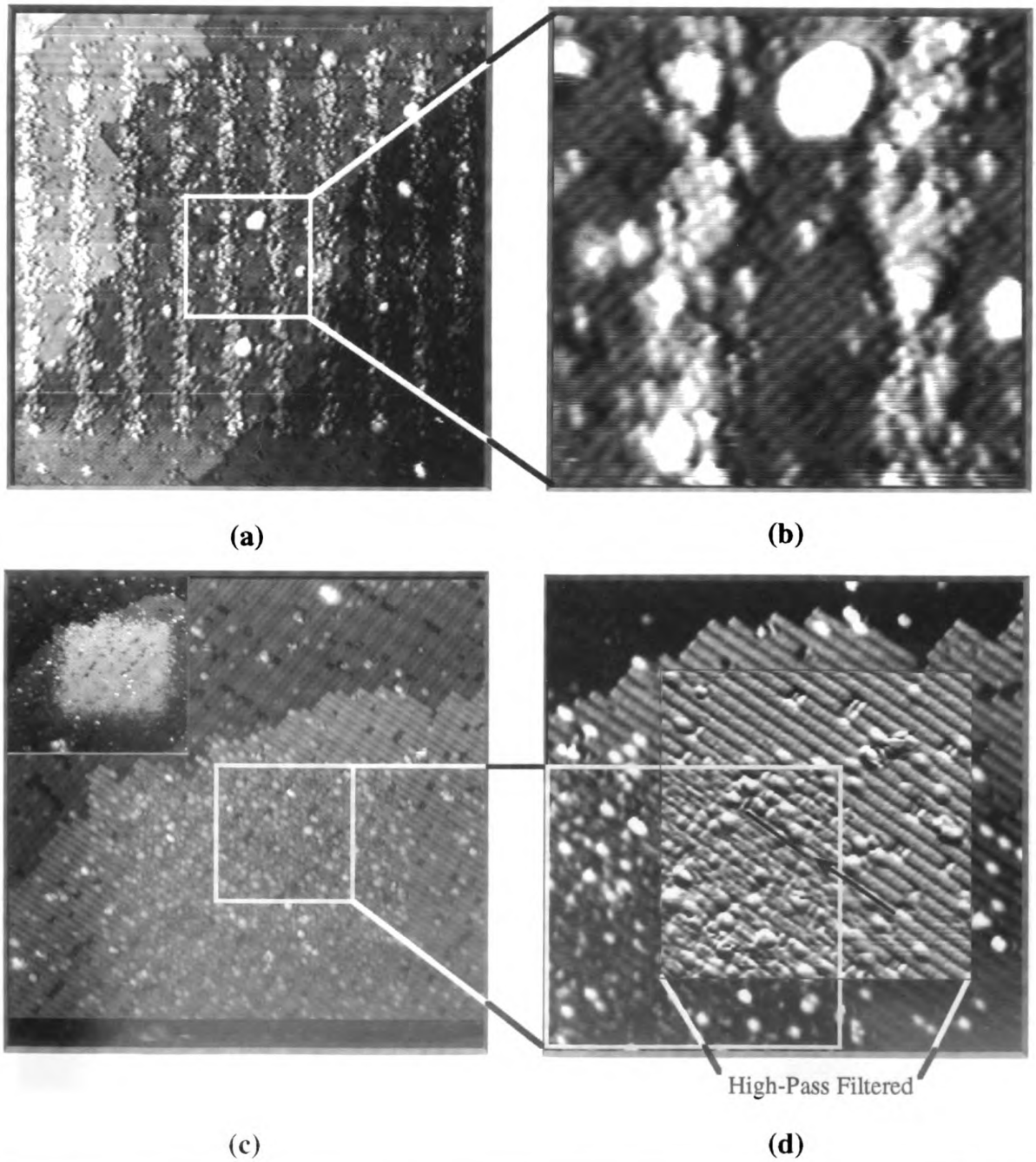
*(a) The desorption yield, atoms/electron, measured from low-dose patterned lines by counting number individual desorption sites and dividing by the number of electrons used to write the pattern. The inset depicts the bonding and antibonding potential energies as a function of separation. (b) Current and voltage dependence of the desorption yield in the vibrational heating regime. The lines represent fits to Avouris' vibrational heating model.*



a closer look, fig. 4d, reveals differences between the H and $NH_3$ passivated regions. By following individual dimer rows across the boundary in fig. 4d it is seen that a node develops down the center of the dimer row only within the $NH_3$ passi-

**Figure 4**

*(a) A 800 Å x 800 Å STM image showing the result of a selective oxidation experiment where the STM patterned sample was exposed to a 100 L [1 L (Langmuir) = $10^{-6}$ Torr sec] dose of $O_2$ while in the UHV chamber. (b) A 200 Å x 200 Å scan of the central region of (a). (c) A 485 Å x 485 Å filled states STM image of a STM patterned area following a 2 L $NH_3$ dose in the UHV chamber. The inset shows the patterned region prior to the dose. (d) A smaller area scan highlighting the differences between the H-passivated and $NH_3$-passivated regions.*



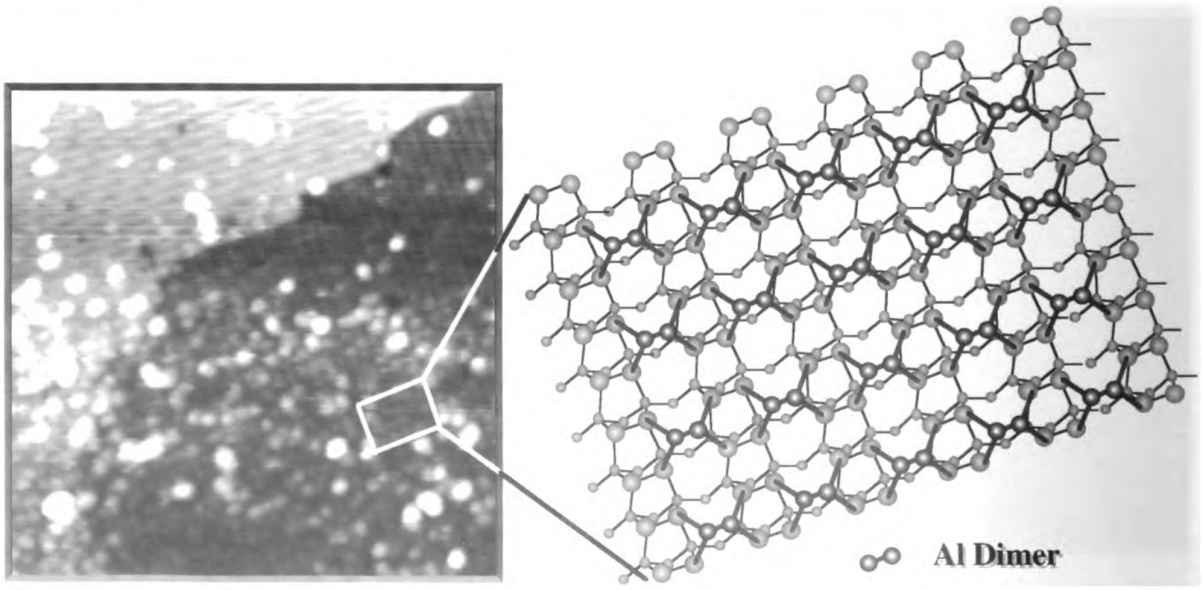
vated region. This node results from the presence of nitrogen which removes electron density from the Si-Si dimer bond and hence appears as a depression in the filled states STM image.

Nanoscale metallization is one of the most important goals for STM nanofabrication. Nearly all future electronic devices will need nanoscale metallization for proper device function and for local interconnects to form circuits. STM-based metallization schemes including field evaporation of metal from the tip[18] and STM assisted dissociation of organometallic precursors[19] have been attempted in recent years. Unfortunately, these methods are limited by sporadic and/or low purity metal deposition. An intriguing new approach to nanoscale metallization is through the use of selective chemical vapor deposition (CVD). CVD metallization techniques are well known and are commonly used in integrated circuit manufacture to make, for example, tungsten via plugs between adjacent layers of metallization. In metal CVD a suitable organometallic precursor molecule reacts with a heated substrate to deposit metal while producing volatile byproducts that evolve from the surface. Unlike physical vapor deposition, this process depends on a chemical reaction, therefore good selectivity and conformal deposition on complex geometries can be achieved by controlling the nature of the surface and the CVD precursor molecule. STM-patterned H-passivated silicon is a good candidate for selective area CVD because of the strong chemical contrast between clean and H-Si. Another attractive feature of this system is the fact that there is no appreciable thermal desorption of hydrogen for temperatures below ~350 °C. The processing temperature window between room temperature and 350 °C is well suited for a wide range of metal CVD precursors.

Fig. 5 shows the result of a thermal CVD experiment on a STM patterned H-Si(100) surface using a novel new aluminum precursor.[20] This experiment was performed at 200 °C with the sample in the STM. The sample was dosed with the metal precursor through a small nozzle connected via a UHV leak valve to an external reservoir of the precursor. From fig. 5a it is seen that the resultant Al deposit is mostly ordered into an overlayer with twice the periodicity (7.7 Å) of the underlying silicon dimer spacing. The diagram in fig. 5b illustrates this ordered overlayer in which Al-Al dimers passivate the dangling bonds of the clean silicon. It is important to note in this experiment that the surrounding H-passivated regions do not react with the CVD precursor. Experiments are now in progress to create metal nanostructures that are connected to macroscopic contacts in order to perform electrical transport measurements. These structures should also enable the atomistic study of electromigration which is an important issue in present day integrated circuit technology.

Much progress has been made in the realm of STM

**Figure 5**
*(a) A 250 Å x 250 Å STM image of a STM patterned H-Si(100) surface showing selective area Al deposition after dosing with a new CVD precursor at 200 °C. (b) A diagram showing the orientation of the Al-Al dimers relative to the underlying silicon.*




(a) (b)

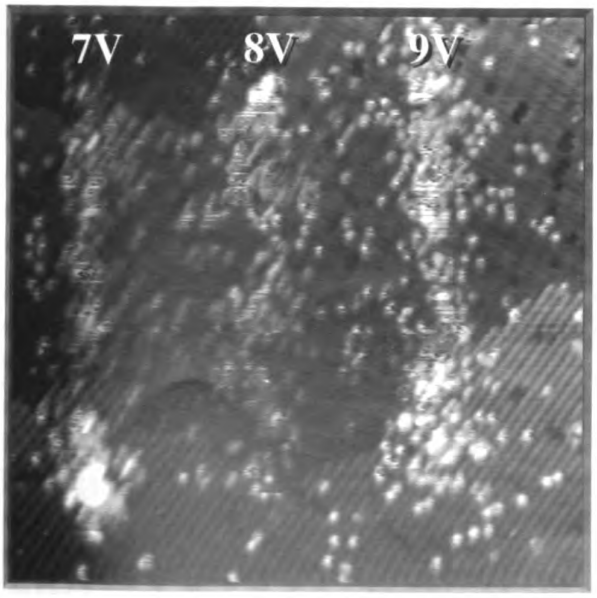
nanofabrication, however numerous challenges still remain. Perhaps the biggest challenge is that of reduction to practice wherein the techniques developed can be applied to the commercial production of tera-scale computer chips. SPM techniques are inherently serial in nature and not conducive to high throughput applications. However, the work by Quate's group at Stanford[21] and by MacDonald's group at Cornell[22], in fabricating parallel arrays of AFM cantilevers and microfabricated STMs, shows great promise towards achieving high throughput lithography tools. In addition to direct write, these tools may also be used to generate masks for technologies such as the nanoimprint technique developed by Chou et al.[23] To that end the UHV STM nanofabrication effort represents the development of optimal processes and device structures for these delivery systems.

# IV. Spin-offs: Deuterium Processing

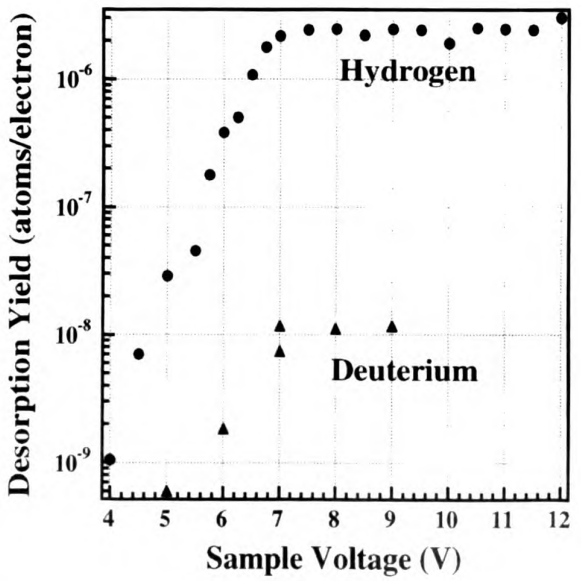
The road to developing nanofabrication techniques for future tera-scale computer and memory storage devices will undoubtedly lead to unexpected discoveries. New and significant information will arise from studies of surfaces, interfaces, and chemical processes at the atomic level. A good example of this is the recent discovery that deuterium processing can be used to dramatically extend the lifetimes of CMOS transistors with regard to hot carrier degradation effects.[3,24] The background for this discovery comes from a set of STM desorption experiments on deuterated Si(100) surface suggested by Avouris.[25] The goal of these experiments was to utilize isotopic substitution to learn more about the mechanisms of hydrogen desorption. Early in these experiments it was discovered that deuterium is approximately two orders of magnitude more difficult to desorb from Si(100) than hydrogen.[1] Fig. 6a shows a representative image in which three lines were patterned on a deuterated Si(100) surface at 7 V, 8V, and 9 V. Sporadic depassivation was observed in this case, and in many others with different tips and samples, under conditions that would completely depassivate H-Si(100) surfaces. Fig. 6b shows the deuterium desorption yield data obtained by analyzing numerous images in this first series of experiments.[1] For comparison purposes, the desorption yield for hydrogen[14] is shown on the same graph. Here it is clearly seen that ~$10^8$ electrons are required to desorb each deuterium atom in the high voltage ESD regime, compared to less than $10^6$ for hydrogen.

The identical shapes of the hydrogen and deuterium desorption yield curves indicate the similarities in the un-

**Figure 6**
*(a) A 450 Å x 450 Å image showing the sporadic depassivation of a deuterium passivated surface under conditions that would fully depassivate H-Si(100). The three lines were patterned at 7 V, 8 V, and 9 V with an electron dose of 1.0 x $10^{-3}$ C/cm. (b) Desorption yield for deuterium compared with that for hydrogen to illustrate the large isotope effect.*




(a)




(b)

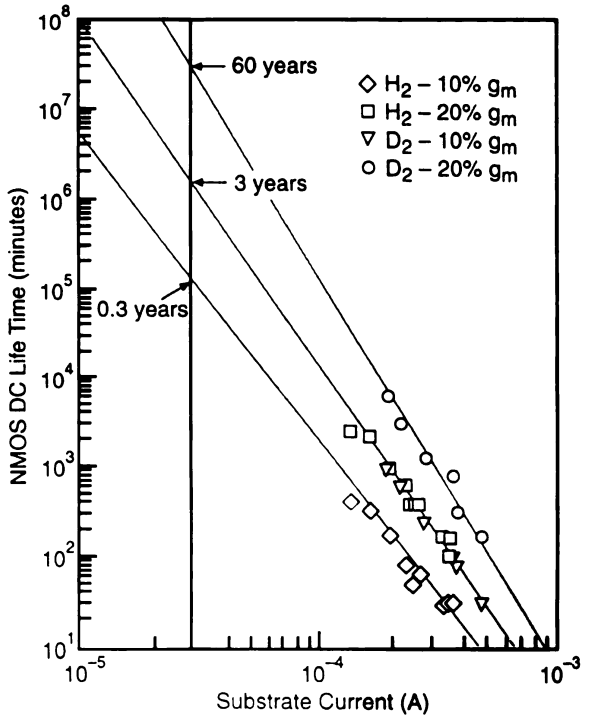
derlying bonding chemistry. However, the dramatic difference in the magnitude of the conversion efficiency results from a large kinetic isotope effect. This behavior is explained by the well known Menzel Gomer Redhead (MGR) effect[26] which describes the differences in desorption between H and D once excitation to the antibonding state has occurred. In the antibonding state the H(D) atom resides in a repulsive potential, acquiring kinetic energy as it accelerates away from the Si surface. Before desorption the H(D) atom usually falls back into the bonding potential and can then escape only if it has acquired sufficient kinetic energy to surmount the bonding potential barrier (see inset in fig. 3a). By a simple classical argument, based on the mass difference, the D atom acquires one-half the kinetic energy for the same excited state lifetime as does the H atom. This reduces the likelihood for deuterium desorption and, in fact, the MGR model predicts an exponential decrease in desorption rate with increasing isotope mass. In addition, this isotope effect is enhanced by the fact that it is more difficult to excite the Si-D bond since its lower vibrational frequency results in better coupling to the substrate phonons. In fact, it has recently been recently pointed out by Van de Walle and Jackson that the vibrational frequency of the Si-D bending mode nearly coincides with one of the silicon phonon modes.[27] This should result in a much stronger de-excitation pathway, decreasing the likelihood of reaching the antibonding state in the first place.

CMOS transistors critically depend on the nature of the interface between their thin gate oxide and the underlying silicon substrate. The highest quality gate oxides are grown by thermally oxidizing the silicon at high temperatures. Due to the molar volume mismatch between the oxide ($SiO_2$) and silicon, however, not all of the silicon ends up bonded to the oxide. This results in dangling bonds at the oxide/silicon interface that number in the range of $10^{11}/cm^2$. During transistor operation these dangling bonds would become charged and scatter conduction electrons as well as shift the voltages used for transistor operation. Since these effects would be intolerable, the semiconductor industry devised a method in the early 1970's using hydrogen to passivate most to the interface dangling bonds.[28] This is accomplished by annealing the silicon wafers in a hydrogen ambient at ~400 °C. At this temperature hydrogen diffuses into the transistors and terminates the dangling bonds at the oxide/silicon interface. While good transistor operation is achieved after hydrogen treatment, it was noticed that transistor properties degrade with time and that this degradation is associated with the reappearance of the dangling bonds at the oxide/silicon interface. The simplest explanation for this degradation is that high energy "hot" electrons flowing along the interface during normal transistor operation stimulate the desorption of the interface hydrogen. By analogy to the STM desorption experiments it became evident that deuterium might be a good candidate to prolong transistor lifetimes in the presence of hot-electrons.[24] This indeed turned out to be the case as learned from tests on CMOS transistors fabricated by Lucent.[3,29] Accelerated stress tests performed on transistors from the same wafer annealed in either hydrogen or deuterium showed lifetime improvements of an order of magnitude or more for the deuterium annealed transistors (see fig. 7). It is interesting to note that there is still a large hydrogen background in the deuterium annealed devices since hydrogen is incorporated during many standard transistor processing steps. Therefore the full extent of the lifetime improvement may not yet be known. It is also important to note that during normal transistor operation the characteristics of hydrogen and deuterium processed transistors are identical since there is no chemical difference between the passivated interface for the two cases.[29] It is only in the presence of hot electrons that the kinetic isotope effect results in a large difference between hydrogen and deuterium processed devices. As a practical matter, the added cost of using deuterium instead of hydrogen amounts to less than $1 US/wafer.

The STM desorption experiments may continue to provide useful information having direct relevance to current

**Figure 7**

*Accelerated stress test results for n-channel MOS transistors annealed in hydrogen and deuterium. By measuring the change in the transistor transconductance, $g_m$, as a function of substrate current it is possible to extrapolate to normal substrate current to predict the actual transistor lifetime. Switching from hydrogen to deuterium shows a factor of 10 lifetime improvement for 10% $g_m$ degradation, and a factor of 20 improvement for 20% $g_m$ degradation.*



and future generations of CMOS based technologies. Although operating voltages are being scaled down along with channel lengths and oxide thickness, it is likely that hot electron degradation effects will continue to play an important role.[30] Consequently, continued STM studies of hydrogen and deuterium desorption from silicon surfaces may yield valuable new information about transistor aging effects. For example, it is possible that vibrational heating might play an important role in the degradation process of CMOS transistors.[31] If this is true then voltage scaling will not eliminate the degradation. Current density is a key factor in vibrational heating and future generations of CMOS will have increased channel current densities. We are now conducting a series of experiments with a variable temperature UHV STM to explore the temperature, current, voltage, and electron dose dependence of hydrogen and deuterium desorption from silicon surfaces.[32] In a series of experiments performed at 11 K it was found that hydrogen is about two orders of magnitude easier to desorb from Si(100) in the vibrational heating regime than at room temperature. This makes qualitative sense, within the context of the vibrational heating model, since the longer wavelength phonons that remain at low temperatures are less effective at quenching the Si-H vibrational modes. Further experiments, combined with detailed modeling, are in progress to fully elucidate the quantitative details. This result does predict, however, that transistors operating at lower voltages and higher current densities may degrade more severely at low temperatures than at room temperature. A recent paper does indeed show increased transistor degradation at low temperatures.[33]

The SPM nanofabrication field is now in a period of rapid growth and diversification. From the development of high throughput practical delivery systems and atomic resolution nanofabrication capabilities has come a variety of new directions, challenges, and unexpected advances.

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# Biography

Joseph W. Lyding is a Professor of Electrical and Computer Engineering at the Beckman Institute of the University of Illinois at Urbana-Champaign. There he established a UHV STM nanofabrication effort and achieved atomic scale patterning of silicon as a basis for developing nanoelectronic devices. His group discovered the deuterium isotope effect which was subsequently found to dramatically harden CMOS transistors against hot-electron degradation. Dr. Lyding is a member of Sigma Xi, AAAS, AVS, APS and IEEE.

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# Cantilever Arrays for Lithography

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## I. Introduction

Martin and Wickramasinghe have assessed the utility of scanning probes in the environment of semiconductor fabrication.[1] They find that "the inherent advantages of AFM and CD-AFM provide new and unique capabilities for accurate metrology in semiconductor development and manufacturing lines." They further state, "Present throughput, in terms of wafers per hour, is still slower by an order of magnitude compared to top of the line SEMs." These instruments may, also, provide a unique capability for lithography provided we can remove the throughput limitation. It is our premise that this can be done with parallel processing of the data which will require arrays of parallel cantilevers each with integrated actuators, sensors, and tips.

In this paper we describe recent progress toward high throughput imaging and lithography using scanning probes. We begin with the work that has been done on increasing the speed of scanning. This first step is necessary in order to reduce the density of probes in the array to a reasonable level of 2 probes/mm$^2$. The area covered by each probe will be $^1/_2$ mm$^2$. If we work with 50 nm pixels and scan this area in 400 seconds, we require a scan velocity of 25 mm/sec. At this speed we would pattern $5\times10^5$ pixels/sec. In order to write data at this rate, the mechanical resonance of the cantilevers would have to exceed 2 MHz.

## II. Integrated Sensors and Actuators

The atomic force microscope (AFM) has proven itself a versatile instrument for science and technology since its introduction in 1986. In spite of the striking advances in the technology of the instrument, the performance is still limited by the serial nature of a single tip scanning at relatively slow speeds over a restricted area. This limitation on data rate and image size is severe. Typically the tip is scanned over an area that is less than 0.01 mm$^2$ with speeds of 10-100 μm/sec. We have shown that these restrictions are lifted

when we use an array of cantilevers with parallel processing.

In conventional AFM operation, the cantilever deflection is monitored with an optical beam precisely aligned to the cantilever, but the task of replicating such a system in an array is difficult. This problem can be obviated using piezoresistive sensors. Individual control of the tip-sample spacing is achieved with piezoelectric actuators. In this section we report our results on imaging with a 2×1 array where the cantilevers are spaced by 100 μm.

Tortonese[2] developed the piezoresistive AFM cantilever as an integrated sensor used for monitoring the cantilever deflection. We have previously used the piezoresistive technology to fabricate and operate an array of five parallel cantilevers for imaging in the constant height mode. In our initial array we scanned the five cantilevers as a single unit with no provision for individual control of the tip-sample spacing. We learned from that experience that individual tip control of this spacing is necessary for imaging in the constant force mode.

Cantilevers with integrated actuators for moving the tips have been developed by several groups,[3] but there are no reports on imaging in the constant force mode with feedback signals controlling the spacing between tip and sample. In many applications we only need individual control for motion along the z-axis (normal to the substrate), since the array can be scanned as a unit in the lateral x-y plane. In such a system, where the piezoresistive sensors provide feedback signals for the piezoelectric actuators, we can image over large areas in the constant force mode.

**Figure 1**
*A SEM micrograph of two parallel AFM cantilevers with integrated piezoresistive silicon sensors and integrated ZnO actuators. Each of the cantilevers is 420 μm in length. The ZnO base occupies 180 μm of the total length. The tips are spaced 100 μm apart, the base of each cantilever is 85 μm wide, and each leg of the cantilevers is 37 μm wide.*

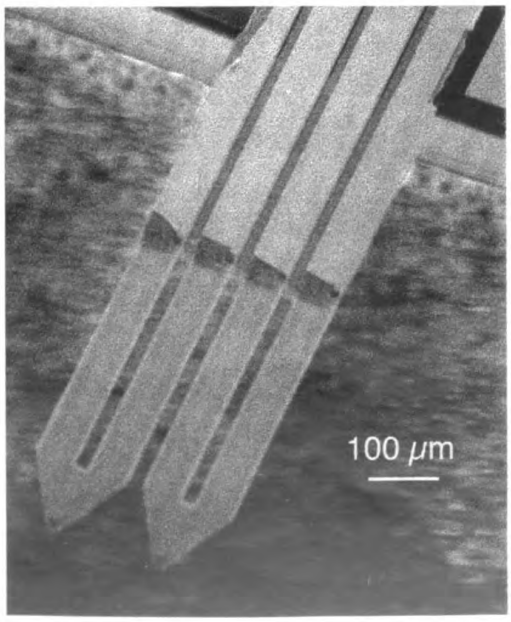
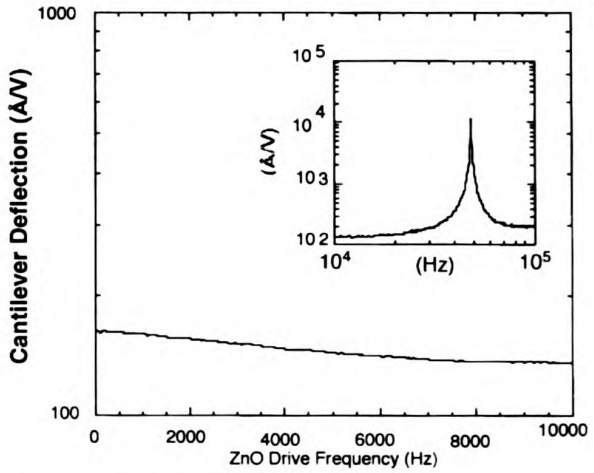



**Figure 2**
*A plot of tip deflection versus ZnO excitation frequency for the cantilevers depicted in Fig. 1. These results were obtained with an optical beam. The DC response is 150 Å/V. The maximum operating voltage on the cantilevers is ± 35 V. The inset shows the response from 10 kHz – 100 kHz. The first resonant peak is clearly seen at 48 kHz.*




A linear array of two cantilevers has been designed and fabricated. Figure 1 shows a typical device: each cantilever is 420 μm in length with the ZnO base region occupying 180 μm of the total length. The full width of each cantilever is 85 μm, each leg of the cantilever is 37 μm in width, and the tips are spaced 100 μm apart. For the device shown in Fig. 1, our analysis, which includes all layers in the structure, predicts a DC deflection of 169 Å/V. The analysis of a uniform system where a single ZnO layer extends the full length of the beam has been carried out by Smits.[4] When his analysis is modified to account for the partial coverage of the beam with the layer of ZnO, it yields a deflection of 196 Å/V. The actual deflection of our device was 153 Å/V (measured optically). Non-uniformity and defects introduced by the fabrication process cause variation in the ZnO response. However, these variations do not restrict imaging because the cantilever is operated in feedback, so constant force can always be maintained. Calibration of an image's vertical scale will depend on ZnO response, and may vary from cantilever to cantilever.

In Figure 2 we display the frequency response for the cantilever shown in Fig. 1. The total deflection of the cantilever is 1 μm for an applied field of ± $10^7$ V/m. For other geometries, we have obtained DC deflections of 577 Å/V which translates to a deflection of 4 μm for voltages of ± 35 V. In Fig. 2 the tip deflection was measured optically.

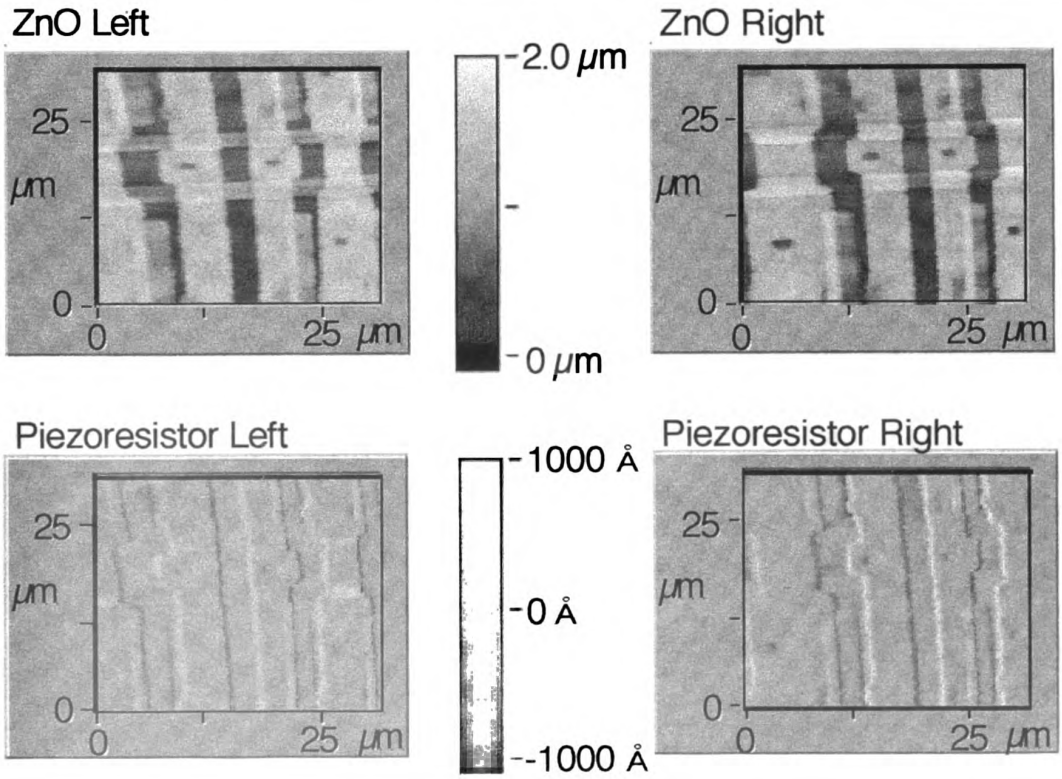
The design of the silicon beam is governed by several factors such as the resonant frequency (20 kHz to 70 kHz) and the spring constants (0.6 to 7.1 N/m). The silicon beam must be thick enough to accommodate the piezoresistor. The piezoelectric film thickness was chosen to maximize the deflection of the silicon beam for a given voltage across the ZnO. For thin ZnO films, the bending force will increase with film thickness, but there is a limit. When the ZnO layer is thick compared to the silicon, the cantilever is merely a slab of ZnO. In this case the applied voltage elongates the beam; it does not bend it. For bending, the ZnO film must be confined to the upper half of the cantilever. In our design the optimum thickness of the ZnO film is equal to the thickness of the silicon beam, 3.5 μm. Since stiffness is proportional to the cantilever thickness cubed, adding the thick ZnO base as an extension to the thin cantilever will have little effect on the spring constant.

The cantilever (or sample) in the conventional AFM is driven with a piezo-ceramic which bends to provide scanning in the lateral plane and extends to control the tip spacing in the z-dimension. Our system, where the stiff ZnO base is used to move the flexible cantilever, is equivalent to the conventional AFM if a laser is used to monitor the deflection. We have used our 2×1 array to acquire simultaneously the multiple images shown in Figure 3. The sample is an integrated circuit chip with 2 μm topography. The ZnO signal records the topography (top images) while the piezoresistor output provides the error signal (bottom images). In the constant force mode the force between tip and sample should remain constant during the imaging cycle. The reduced height scale for the error signal of Fig. 3 indicates that this condition has been satisfied.

One common limitation of the AFM is the amount of time required to image surface areas on the micron scale. Scan speeds in the constant force mode are typically limited to less than 200 μm/s because of the poor mechanical response of piezo tubes used to scan a sample. At this rate, a single 256 × 256 pixel image of a 50 × 50 $\mu m^2$ area takes a few minutes to acquire. Furthermore, if the cantilever deflection signal contains frequencies above the lowest resonance of the piezo tube, large shifts in phase within the feedback loop cause the system to become unstable, and the tip/sample force will no longer be constant.

We have found that tip velocities can be increased by over an order of magnitude by using the integrated ZnO actuator rather than a standard piezo tube to achieve constant

**Figure 3**
*Parallel constant force images taken with a 2×1 array of ZnO cantilevers. The ZnO signal represents the final image. The piezoresistive signals represent the error signals. Constant force imaging can be seen by the flatness of the error signal and the positive and negative shifts at the grating step edges.*



force. The open-loop frequency response of this system is shown in Figure 4a. The resonance of the cantilever when in contact with the sample surface is near 44 kHz. Also shown in Fig. 4a is the response of a 2-inch piezo tube, a commonly used size for applications requiring scans up to 100 μm. The sharp peak near 600 Hz is associated with a lower resonance of the piezo tube.

An image of an integrated circuit taken with a tip velocity of 3 mm/s in the constant force mode is shown in Fig. 4b. The integrated circuit consists of metal lines and contact holes and contains vertical steps 2 μm in height. The ZnO drive signal required to bend the cantilever over the sample topography was under ±30 V. The sample was imaged by raster scanning over a 30 μm × 30 μm area using a 1-inch-long piezo tube with a fast scan rate of 50 Hz. The high resolution image of 512 × 512 pixels was acquired in roughly 15 seconds. The fast visual feedback with this scanning rate makes it easy to adjust parameters such as position, zoom, and rotation—similar to what is available with an SEM.

In summary, we have demonstrated that batch fabricated cantilevers can be used as a parallel array for an AFM operating in the constant force mode. The individual cantilevers can be deflected through 4 μm with a minimum detectable deflection of 22 Å over a 10 Hz – 1 kHz bandwidth. The integrated actuators allow high speed scanning. Real time imaging with the AFM is useful since it reduces the time required to search for a selected feature on the sample. More importantly, the ability to scan at high speeds and with control of individual tips in a parallel array is essential for increasing the throughput of scanning probe lithography and data storage systems.

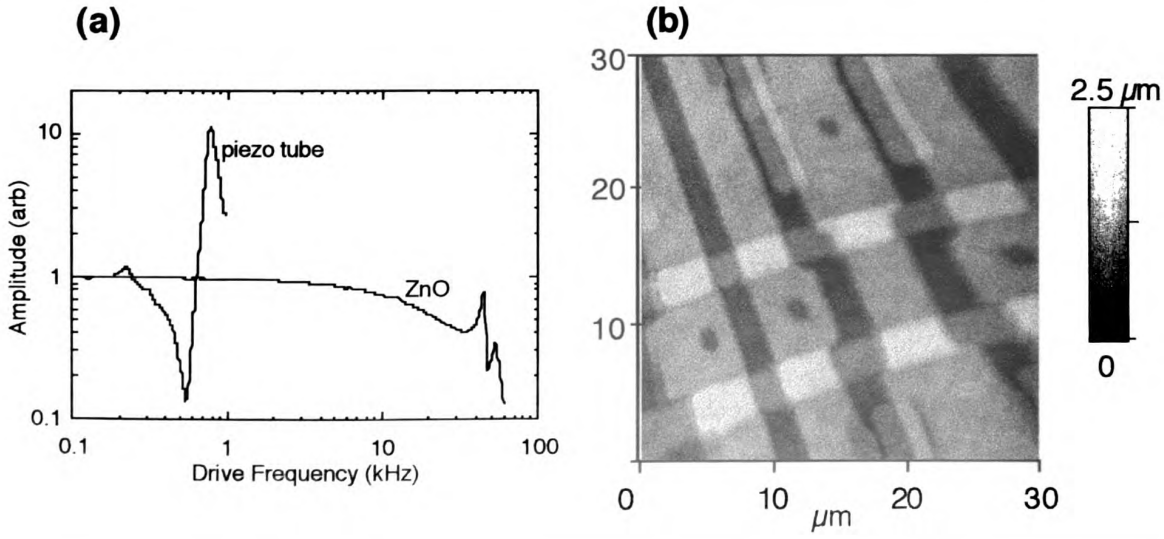
# III. Optical Sensors Suitable for Arrays

An alternate approach for imaging with arrays is to measure the deflection of each cantilever optically rather than using the piezoresistor. To obtain maximum sensitivity for imaging, the circuitry used to measure the cantilever deflection should be located as close as possible to the deflection sensor. In the case of the piezoresistor, this circuitry consists of a resistive bridge and a high quality amplifier. Incorporating these elements, along with the necessary electrical connections, close to the piezoresistor increases the fabrication process complexity.

In the case of an optical system, the detection circuitry would not need to be placed on the cantilever chip. In addition to simplifying the array fabrication process, the external circuitry reduces the number of bond pads per cantilever thereby allowing the array density to be increased. The optical detection system would also eliminate electrical coupling from the actuator and lithography signals to the deflection signal.

One of the most sensitive optical techniques for measuring the deflection of a cantilever is the interferometer. Rugar, *et al.*,[5] developed a deflection sensor based on the

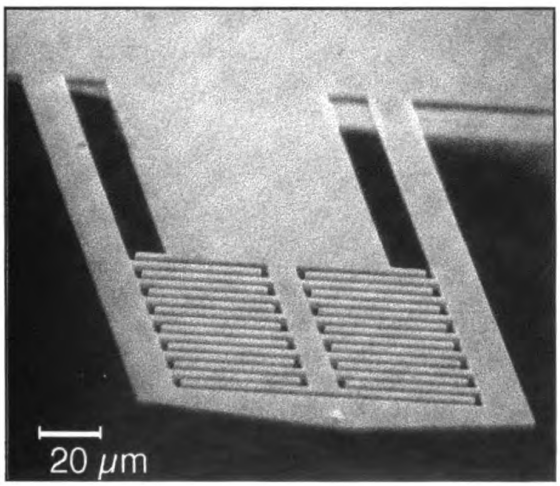
**Figure 4**
*a) Amplitude response of the piezoresistor as a function of the frequency of the ZnO actuator. Shown for comparison is the response of the cantilever driven with a 2-inch piezo tube. b) Image of an integrated circuit scanned at a tip velocity of 3 mm/s.*



interference of light between the cleaved end of an optical fiber and the backside of a cantilever. By accurately positioning the fiber above the cantilever to form a tightly spaced interference cavity of less than 4 μm, it is possible to achieve a vertical resolution on the order of 0.01 Å.

The process of optically measuring deflection can be simplified through a technique known as the optical lever.[6,7] In this system, a laser beam is reflected off the backside of the cantilever and directed into a split photodiode. The position of the reflected beam, and hence the cantilever deflection, is determined by subtracting the photodiode outputs. Unlike the interferometer, the optical lever does not require the positioning of components directly above the cantilever. It is this simplicity that has made the optical lever more popular than the interferometer. However, applying the optical lever to cantilever arrays could require strict alignment requirements of the photodetectors.

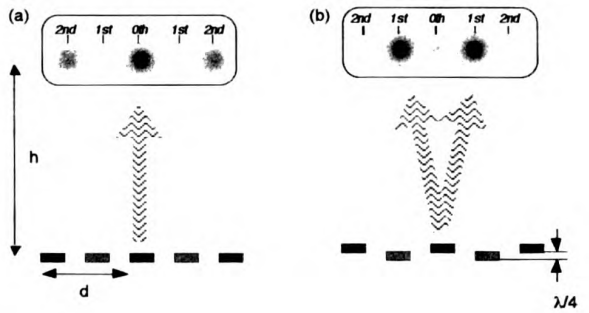
**Figure 5**
*SEM micrograph of an interdigital cantilever that is 215 μm long, 2.5 μm thick, and contains 3-μm-wide fingers.*




A more practical approach is to micromachine a cantilever into the shape of interdigitated fingers to form a diffraction grating (see Figure 5). When a force is applied at the tip, alternating fingers are displaced while remaining fingers are held fixed. This creates a phase sensitive diffraction grating, allowing the cantilever displacement to be determined by measuring the intensity of diffracted modes. We have found that this cantilever can be used with a standard AFM without modification and achieve a sensitivity of 0.02 Å in a 1 kHz bandwidth. Most importantly, the interdigital cantilever alleviates the task of critically aligning an array of photodiodes since intensity rather than position of the reflected beam is measured.

The operation of the interdigital cantilever is schematically depicted in Figure 6 where the diffraction pattern is

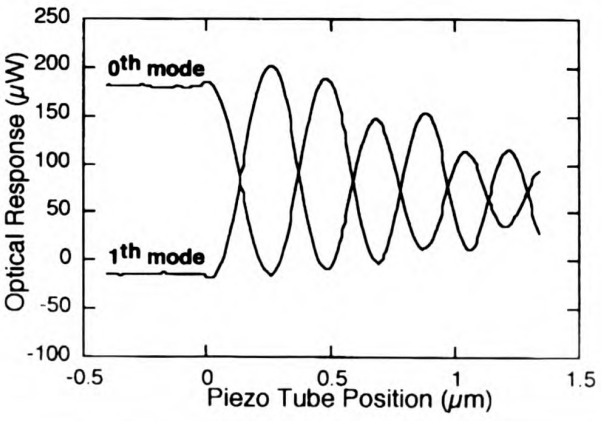
**Figure 6**
*Schematic operation of the interdigital cantilever.*




numerically calculated using a far field approximation at a vertical position, h, above a cantilever with a diffraction period, d. The cantilever is illuminated with a Gaussian beam with a diameter of 20 μm and a wavelength of λ=670 nm. A cross-section of the interdigitated fingers is shown at the bottom of Fig. 6 to indicate the cantilever deflection. In Fig. 6a, the cantilever is not deflected and the dominant reflected beam is the 0th mode. As the tip is displaced by an external force, the interference between the light reflecting off the reference fingers (dark) and the moving fingers (gray) causes the 0th mode intensity to decrease while a 1st mode is created. When the cantilever has deflected by an amount of λ/4, where λ is the wavelength of the illumination source, the 0th mode is minimized and the 1st mode is maximized (see Fig. 6b). The cantilever deflection can be determined by either measuring the intensity of the 0th mode, 1st mode, or the difference between the modes. The distance between the 0th and 1st mode is equal to $h \times \lambda/d$ and is roughly 2 mm for our system.

Figure 7 shows a typical force curve that is obtained

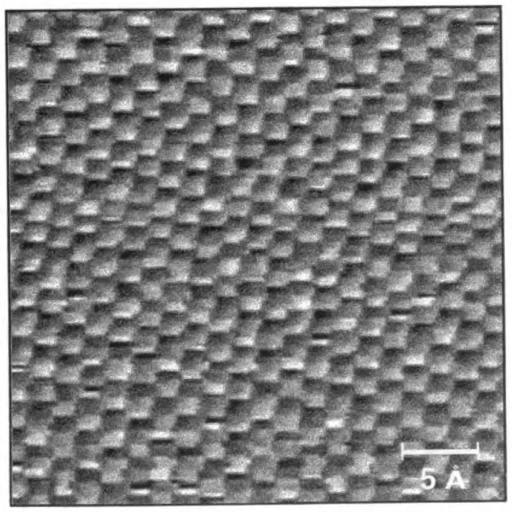
**Figure 7**
*Interdigital force curve*



by measuring the intensity of the 0th or 1st order modes as a function of cantilever deflection. A laser diode with a wavelength of 670 nm is focused to a ~20 μm spot and aligned to a set of interdigitated fingers. The intensity of the diffracted modes is measured with a split photodiode placed roughly 4 cm from the cantilever.

An atomic image of graphite acquired with the interdigital cantilever is shown in Figure 8. The square-like quality of the atoms results from a relatively large contact force between the tip and sample. To maximize sensitivity, the outer portion of the cantilever must be deflected, or biased, by applying a force at the tip. This is undesirable because it is not possible to arbitrarily choose the tip/sample force while maintaining maximal sensitivity. In future generations of the interdigital cantilever, we plan to bias the deflection of the reference plane in the fabrication process such that maximum sensitivity is achieved without adjusting the deflection of the outer portion of the cantilever.

**Figure 8**
*Atomic image of graphite.*




Arrays of interdigital cantilevers can be operated in parallel by using a cylindrically focused laser for illumination and an array of silicon photodetectors to measure the 0th, 1st, or both modes from each cantilever. Photodetector arrays consisting of 512 elements with a 50 μm pitch that contain integrated electronics are commercially available.

# IV. Oxidation of Amorphous Silicon

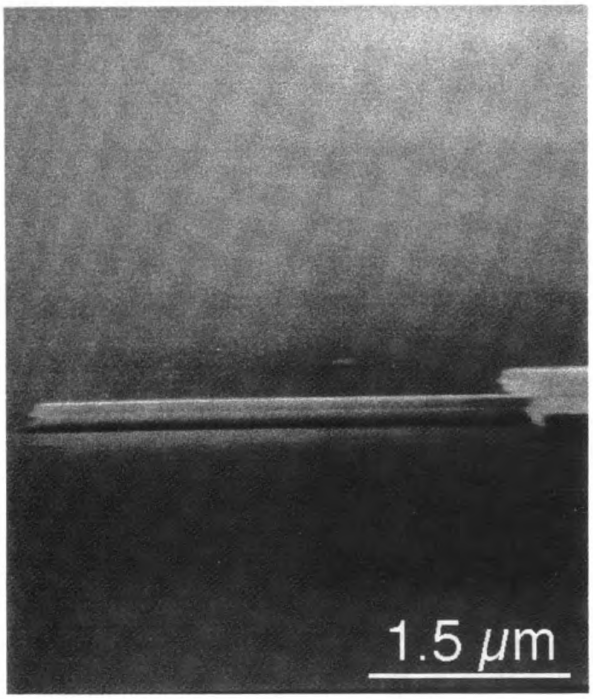
Scanning probe lithography (SPL)[8] has recently gained popularity because device feature sizes in integrated circuits are approaching the optical diffraction limit. For SPL to be accepted as a lithographic tool in the deep sub-micron regime, it must be able to pattern arbitrary surfaces in a manner that is compatible with clean room processes. Using amorphous silicon (α:Si) as a resist provides a way to lithograph general surfaces in both the positive and negative tone.

Single tip SPL began with Dagata[9] on hydrogen passivated (111) single crystal silicon. Lyding,[10] Snow,[11] and Campbell[12] have made further advances by using the STM and AFM to pattern other orientations of silicon. The mechanism for this type of lithography is presumed to be that the intense field from the tip desorbs the hydrogen and increases the oxidation rate on the exposed silicon. An oxide pattern formed in this manner can serve as an etch mask for transferring the pattern into the silicon substrate. Lyding has shown that the STM oxidized linewidth can be as small as 15 Å.

SPL has been limited in that only certain surfaces can be directly patterned. Sugimura[13] used the scanning tunneling microscope (STM) to selectively oxidize metal films. Majumdar[14] used the AFM to expose thin layers of PMMA with electrons from a conducting tip, and Mamin[15] used the AFM to thermomechanically modify PMMA. Sohn[16] fabricated metallic nanostructures using the AFM. He used the probe tip to plow through the top resist layer and subsequently developed the resist to create a mask through which metal can be deposited. Although these techniques are useful in certain applications, it is desirable to pattern arbitrary surfaces. For this reason we prefer the lithography system of selectively oxidizing amorphous silicon as discussed by Kramer.[17] Amorphous silicon is advantageous because it is compatible with semiconductor processing, it can be deposited in thin films, and it can serve as an etch mask to many materials.

Snow and Campbell replaced the conducting probe of the STM with a titanium coated nitride cantilever and performed electric field enhanced oxidation with the AFM. In our work we used two types of cantilevers. For lithography with silicon nitride cantilevers, we evaporated 300 Å of titanium on to the cantilevers to form the conducting path. Our work with piezoresistive silicon probes uses the technology developed by Tortonese[2] at Stanford. Electrical connection to the tip in a piezoresistive cantilever can be easily implemented; the piezoresistor's duty need only be changed from a sensor to a conducting path. Although the piezoresistor's duty can be toggled depending on the mode of operation of the AFM, we dedicated the piezoresistor to lithography and imaged using the Park Scientific Instrument "Universal"

**Figure 9**
*A released cantilever structure created by AFM lithography. The 1000 Å α:Si structure rests on 5000 Å thermal oxide. The cantilever was undercut in 6:1 buffered oxide etch. The cantilever shown is 350 μm long, 0.4 μm wide and 1000 Å thick. The cantilever pedestal is 5 μm by 5 μm. The gap between the cantilever and the substrate is 1500 Å. The viewing angle is 85 degrees.*




commercial laser deflection system. During our fabrication of the piezoresistive cantilevers, a 300 Å protective oxide was grown over the final tip structure. This insulating layer was removed in 10:1 buffered oxide etch for lithographic applications.

Combining Kramer's patterning of α:Si films and Snow's work on suspended silicon structures, we deposited 1000 Å of low pressure chemical vapor deposition (LPCVD) α:Si at 400 mT, 560°C, and a 1.24:1 $SiH_4$:$H_2$ gas ratio onto 5000 Å of thermal oxide. By patterning the α:Si into the shape of a cantilever and using the field induced oxide as an etch mask, we defined the cantilever structure in α:Si. The α:Si is etched in a 1:1 $SF_6$:Freon 115 plasma at 150 mT and 0.22 W/cm$^2$. By undercutting the cantilever in a 6:1 buffered oxide etch, we fabricated a free standing α:Si structure shown in Figure 9. The cantilever shown is 350 μm long, 0.4 μm wide and 1000 Å thick. The cantilever pedestal is 5 μm by 5 μm. The gap between the cantilever and the substrate is 1500 Å. The viewing angle is 85 degrees.

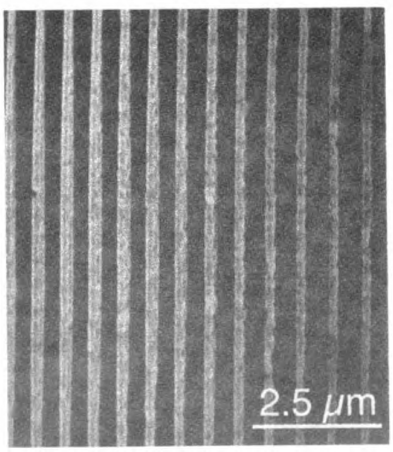
A general form of resist for AFM lithography can be implemented by using the α:Si structure as an etch mask instead of the final feature. A 1000 Å α:Si film on 5000 Å of oxide was prepared by the same method described above. Lines were lithographed in parallel by silicon nitride cantilevers coated with 300 Å of titanium with the AFM at 0.5 μm/s. Each line was created with two passes of the tip (one in each direction). The lithographed pattern was transferred into the α:Si in the same $SF_6$:Freon 115 plasma. The pattern was then transferred into the 5000 Å of oxide by reactive ion etching. The dielectric etch was performed at a DC bias of -530 V, power density of 0.95 W/cm$^2$, gas mixture of 14.2:1 Freon 23:$O_2$, and pressure of 250 mT. Figure 10 shows the resulting lithography on oxide where the line on the left was patterned at 25 V with the voltage decreasing by 1 V for each line to the right. The linewidth decreases from 0.25 μm at 25 V to 0.16 μm at 13 V.

The transfer of the patterned lines into the oxide in Figure 10 becomes incomplete at higher scan speeds. It is due to limited etch selectivity; if the field induced oxide is not thick enough to withstand the entire α:Si etch, it will not be able to mask the entire thickness of α:Si. Likewise, if the remaining α:Si is not thick enough to withstand the entire substrate etch, complete pattern transfer will not be obtainable. In general:

Maximum Substrate Etch Depth =
AFM Induced Oxide Thickness
× Selectivity of the α:Si Etch Against Oxide
× Selectivity of the Substrate Etch Against α:Si

Etching beyond this limit provides no further relief to the lithographed pattern because the masking material has been completely etched. This limit can be circumvented by inserting an intermediate layer that has a high selectivity

**Figure 10**
*5000 Å of thermal oxide patterned with an α:Si mask which was lithographed by the AFM. Lithography on the α:Si occurred at 0.5 μm/s. The line on the left was lithographed at 25 V; each line to the right was lithographed at one less volt.*



against the substrate etch, and its etch has a high selectivity against α:Si. Inserting such a material makes complete pattern transfer easily obtainable using an α:Si mask.

AFM lithography using a chromium intermediate layer is shown in Figure 11. On a (100) silicon wafer 9500 Å of thermal oxide, 3500 Å of LPCVD nitride, 1500 Å of evaporated chromium, and 3500 Å of evaporated α:Si were deposited in sequence. AFM lithography and α:Si pattern transfer were performed in the same manner as before, leaving the chromium layer partially exposed (Fig. 11a). The chromium was then etched in a commercial chromium wet etch exposing the nitride. The nitride was RIE etched in $NF_3$ (dc bias = -200 V, power density = 0.46 W/cm$^2$, and pressure = 60 mT) and oxide below was then etched in the dielectric etch mentioned previously (Fig. 11b and 11c). The α:Si masking layer was removed in the nitride etch (selectivity = 2 : 1 α:Si : Ni). However, because these etches do not significantly attack chromium, the intermediate masking layer remained undisturbed. The pattern was then transferred 3 μm into the silicon in an isotropic silicon etch. Figure 11d shows the masking layer still completely intact after trans-

**Figure 11**

*AFM lithography using a compound α:Si/chromium resist. a) Parallel pattern transferred into 3500 Å of α:Si. The material in the background is 1500 Å of chromium. b) The lithographed pattern transferred into 3500 Å of silicon nitride and 9500 Å of silicon dioxide. The α:Si masking layer is completely removed, exposing the chromium. c) Close up of a 0.3 μm line. d) The pattern is transferred into 3 μm of the silicon substrate. The chromium masking layer is intact.*

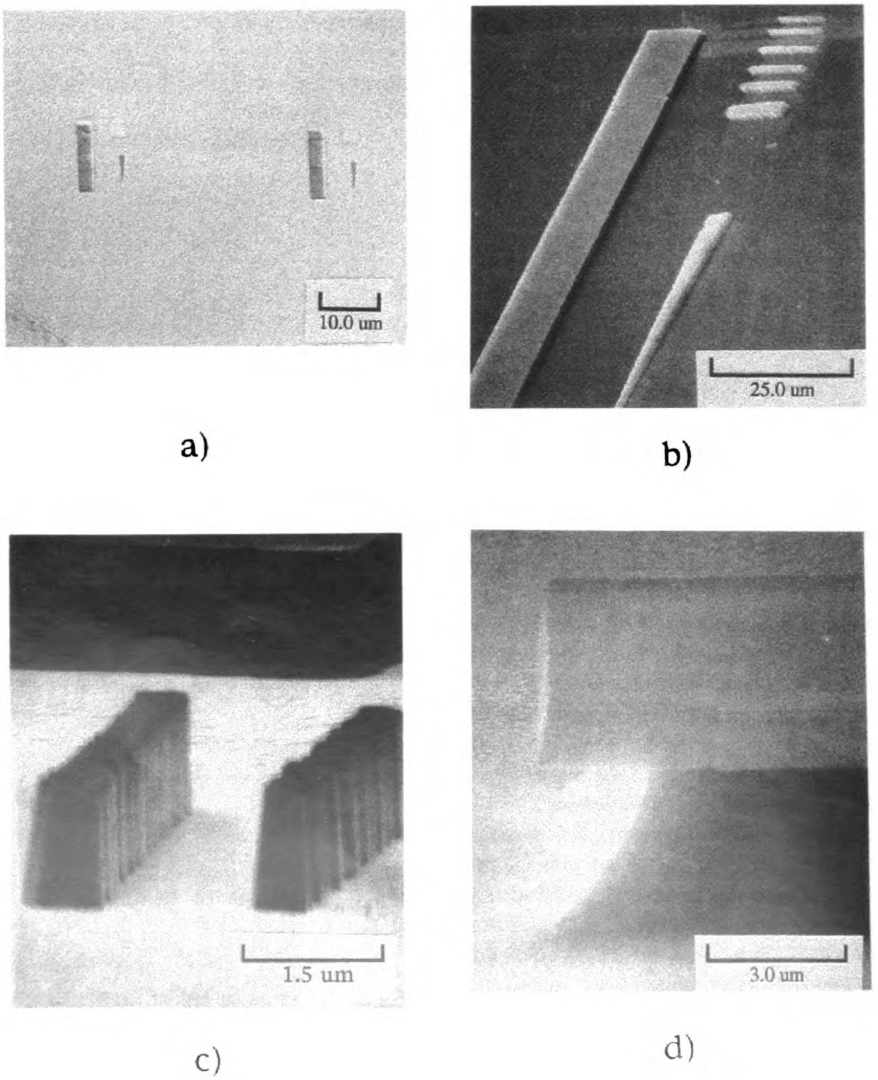
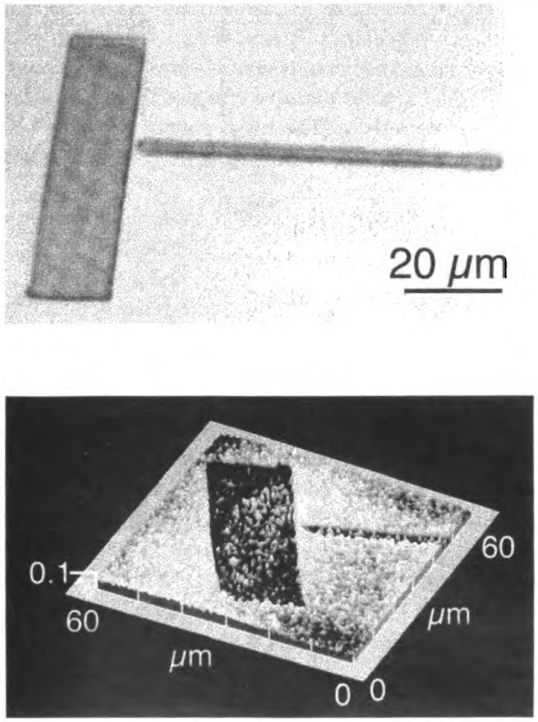


**Figure 12**
*Illustrations of α:Si used in conjunction with titanium to form a positive resist. a) 3500 Å of α:Si patterned on 1500 Å of titanium. The background titanium has oxidized from exposure to air, the titanium underneath the amorphous is protected from oxidation. b) AFM image showing a positive tone transfer into the silicon substrate; the pattern depth is 400 Å. Black areas in the AFM image correspond to depressions in the surface.*




ferring through of 4.5 μm chromium, nitride, oxide, and silicon in four different etches.

So far we have only used α:Si as a negative resist, hence what was exposed with the AFM remains during development (etching). In many instances it would be more convenient to have a positive resist, which would result in exposed areas being removed during development (etching). By exploiting the difference in etch rate between α:Si and titanium oxide, titanium/α:Si can be used as a positive resist as it is shown in Figure 12. On a (100) silicon wafer we deposited 1500 Å of titanium by evaporation, then without breaking vacuum, we immediately deposited 3500 Å of amorphous silicon. When the sample was removed from the evaporator, the α:Si film protected the titanium from oxidizing. AFM lithography was performed and the pattern was transferred into the α:Si, partially exposing the titanium surface (Figure 12a). The exposure of the titanium surface to air formed a native oxide on the titanium in the regions that were not protected by the α:Si pattern. We then etched the surface in a 1:1 $SF_6$:$CF_3Br$ plasma at 150 mT and 0.81 W/cm$^2$. This etch attacked titanium, titanium oxide, and α:Si, but all at different rates. The differential etch rate between titanium oxide and α:Si is such that the entire α:Si layer is etched before the native titanium oxide. Once the α:Si is completely removed, the unoxidized titanium beneath is quickly attacked. The titanium which was not masked by the α:Si was still protected by the native oxide. The resulting titanium pattern was then used as an etch mask to transfer the pattern 400 Å into the silicon substrate (Fig. 12b).

# V. Lithography Over Topography

In many real patterning applications, such as integrated circuit lithography, samples may have significant topography. Patterning over topography is a challenge for most forms of lithography. Organic resists spun on a wafer with topography tend to planarize, resulting in resist thickness variations across the sample. In photolithography, this causes linewidth variations across the wafer due to scattering of light off the topography and to the interference effect.[18] The resist thickness may in fact exceed the system's depth of focus in certain regions, particularly for high resolution lithography. It is also difficult to achieve uniform patterns over topography using electron beam (e-beams) lithography. This is a result of electrons backscattering from the substrate and changing the feature profile near a topographic step.[19] Early SPL studies have been limited primarily to demonstrations of the technique's fine resolution. Little work has been done to address the challenges of real patterning applications, such as that of patterning over topography. Here we describe our studies of scanning probe lithography over topography using two different SPL methods: selective oxidation of α:Si and the electron exposure of an organic resist.

We used the method of α:Si local oxidation described in Section IV to pattern the critical gate level of a metal oxide semiconductor field-effect transistor (MOSFET). All other levels were patterned with conventional photolithography. The transistor was fabricated with a simplified four-mask process which started with a (100) *p*-type silicon wafer with a resistivity of 10-20 Ω-cm. The first step was the growth of a half micron layer of thermal oxide, called the "field oxide." We next opened a window in this layer by removing the field oxide over a rectangular area measuring 70 × 30 μm. This area is called the "active region." The gate oxide was grown to a thickness of 87 Å and then 1000 Å of α:Si was deposited by low-pressure chemical vapor deposition (LPCVD). The α:Si deposits conformally on the existing oxide topography. It is this α:Si that we need to pattern with the AFM to create the transistor gate.

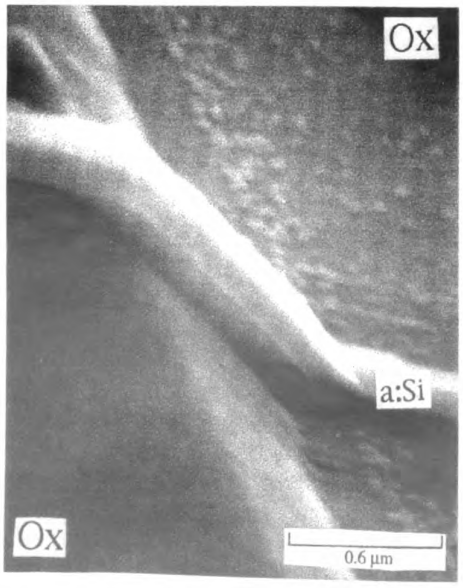
We hydrogen passivated the α:Si film by submersing the wafer in a 5:1 $H_2O$:HF solution for 4 min. The sample

was then loaded into a standard Park Scientific Instruments AFM equipped with a silicon nitride cantilever coated with 300 Å of titanium. The AFM was used initially to image the transistor structure and determine the proper location to write the gate. We then applied a 12 V bias to the α:Si while grounding the tip and moved the probe across the active area at a speed of 0.55 μm/s. This created an oxide line 33 Å high and 0.21 μm wide. The AFM-induced oxide pattern was next transferred into the α:Si by 1:1 $SF_6$:Freon 115 plasma. The etching of the α:Si was monitored by laser interferometry, and the etch was terminated when the α:Si was completely etched.

We found that if the step edge between the active and field area is abrupt, the tip can pull off the surface. This results in a break of the line, which would make the transistor fail. Since the oxide line can be imaged immediately after patterning, this could be used to detect defects or breaks. Another solution is to create a more gradual step that the tip can easily follow. We used an isotropic etch to grade the oxide step between the field oxide and the gate oxide. Figure 13 is a SEM micrograph of the continuous etched α:Si line traversing the oxide step edge. Using this method for gate lithography, we successfully fabricated an *n*MOSFET with an effective channel length of 0.11 μm. The electrical characteristics were reasonable with a transconductance of 279 mS/mm and a threshold voltage of 0.55 V.

This local oxidation process is powerful because of the fine resolution and the resistant oxide etch mask that is created. Patterning is slow, however, limited by the reaction rate at the surface. Writing speeds are under 10 μm/s, making patterning of finite areas in reasonable times unmanageable. Local oxidation also results in significant tip wear.

**Figure 13**
*SEM micrograph of the α:Si gate passing over the oxide step that separates the field and gate regions.*



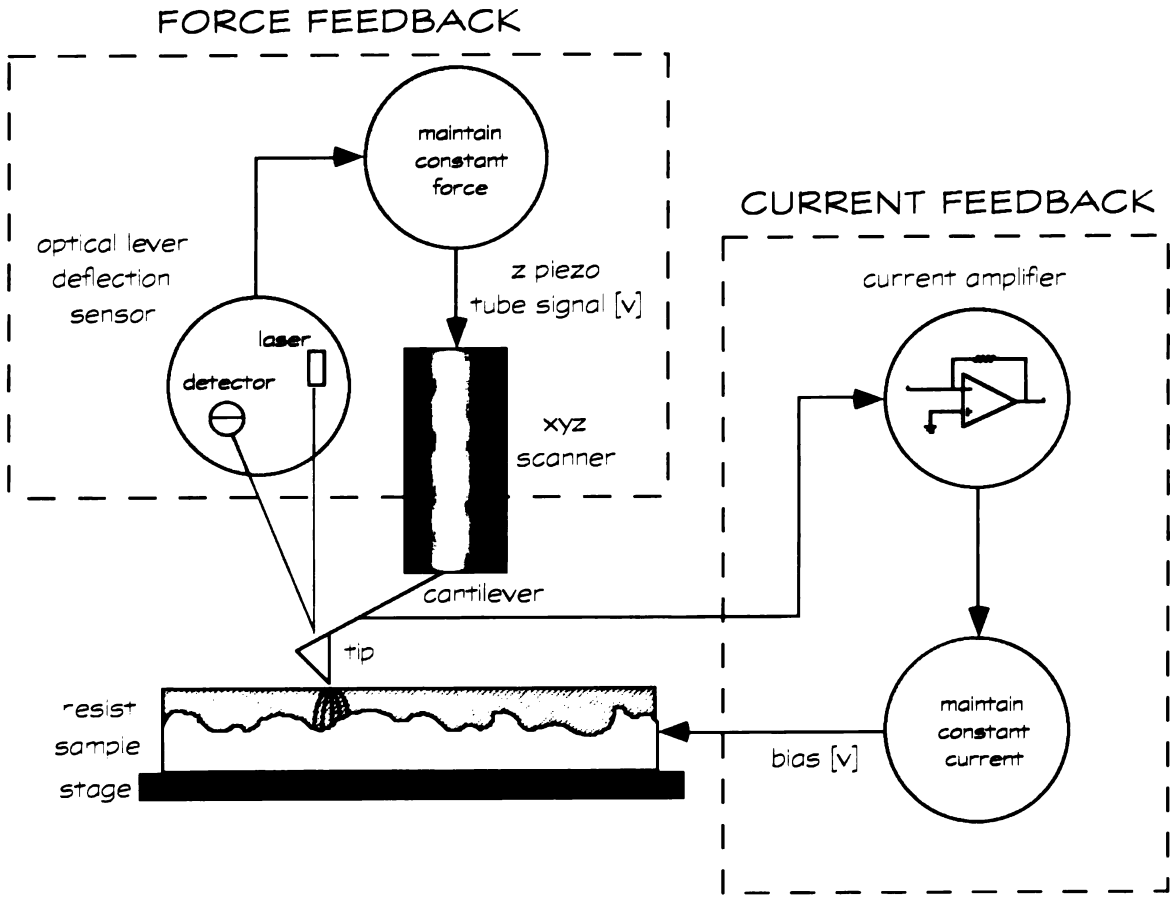

Another scheme for performing lithography with scanning probes involves the electron exposure of a resist material, such as an organic polymer or a monolayer resist. When a conducting tip is biased negatively with respect to a sample, electrons are field-emitted from the tip. If a sample is coated with a thin resist, the emitted electrons traverse the resist. The resist absorbs energy from the electron radiation, which induces chemical changes in the resist. For organic polymer resists, the radiation scissions bonds (positive resist) or crosslinks molecules (negative resist). As a result, when the resist is submersed in a special solvent (the developer), only the irradiated areas dissolve (for positive resists; opposite for negative resists). The resist pattern can then be transferred to the substrate using selective chemical etching or dry etching.

Organic polymer resists provide an attractive option for SPL because many have a low threshold voltage, high sensitivity, sub-100-nm resolution, and good dry etch resistance. Moreover, these resists can be easily deposited on virtually any substrate, and many organic polymers are well characterized from use in photolithography or e-beam lithography. It is also possible to pattern at higher speeds with this method. Finally, the polymer surface is soft and pliable which should significantly reduce the tip wear.

Both the STM and the AFM have been used to pattern organic polymer resists. In STM lithography, a fixed tip-sample bias is applied and the spacing is varied to maintain a constant current through the resist.[20] This system, however, suffers from poor alignment capabilities (imaging may expose the resist). It is also tricky to determine the appropriate voltage bias for STM lithography. If the bias is set too high, the tip may move far from the sample resulting in beam spreading. If the bias is too low, the tip may in fact penetrate the resist in an attempt to achieve the setpoint current.[21] These factors make STM lithography of organic resists problematic. In AFM lithography, the force between the tip and resist is held constant while a fixed voltage bias is applied to generate the field-emitted current.[22] Constant-voltage operation is not ideal since the required voltage is a strong function of the tip and sample materials, the tip shape, and the resist thickness. Therefore if the tip shape or resist thickness changes, for instance, the dose of electrons delivered to the resist will change. This could result in non-uniform or unrepeatable patterns. These issues would also make it difficult to extend STM or AFM lithography to reliable multiple probe patterning.

For the reasons given above, it is impractical to pattern an organic resist spun over topography with either the STM or the AFM. In STM lithography, the problem is usually one of beam spreading causing linewidth variations between regions. A more aggressive attempt to limit beam spreading can cause the tip to penetrate the resist in the thicker regions. With the AFM, the chosen bias will likely pattern

**Figure 14**
*Schematic diagram of the Hybrid AFM / STM lithography system incorporating dual feedback loops, one to maintain a constant force between the tip and sample and the other to keep a constant field-emission current through the resist.*




only one region (perhaps only the thinner resist), but not expose another region at all.

We have designed a new scanning probe lithography system to circumvent these problems. The Hybrid AFM / STM lithography system combines the key features of the AFM and STM by incorporating two independent feedback loops (Figure 14). One loop maintains a constant small force (typically 10 nN) between the tip and the electron-sensitive resist, thereby minimizing the beam spreading that limits the resolution of STM lithography. The force is detected by monitoring the cantilever deflection with a conventional optical lever beam-bounce system. A signal is sent to the piezo tube actuator to move the probe up or down to maintain the setpoint force.

The other feedback loop maintains a constant field emission current through the resist during exposure (generally in the range of 20 pA to 1 nA). The current through the resist is measured with picoAmpere sensitivity using a commercial current preamplifier. The current is measured at the tip for lowest noise operation. The feedback circuit compares the measured current to the setpoint current. A high voltage amplifier applies the necessary voltage to the sample (generally 20-100 V) to maintain the setpoint current.

We have found that the critical parameter for exposing an organic polymer with scanning probes is the dose of electrons delivered to the resist. In the case of SPL, the line dose (in Coulombs/cm) is the ratio of the current to the writing speed. The width of the exposed region depends critically on this line dose, which can be easily specified using the Hybrid AFM / STM system. The smallest lines we have patterned are 41 nm at a line dose of 26 nC/cm. Features can be patterned at higher speeds by increasing the current proportionally. Because of the current sensitivity on voltage, current can be increased by orders of magnitude with only a

few volts change. Therefore this patterning technique can be extended to higher speed patterning. We have patterned at speeds up to 200 μm/s and foresee no physical speed limitations to this patterning mechanism within reasonable scan speeds.

The Hybrid AFM / STM system delivers a constant dose of electrons everywhere while maintaining a minimum tip-sample spacing. This should allow patterning of continuous and uniform features over topography where the resist thickness changes as a function of position. We will use this system to pattern the gate of a 100-nm *p*MOSFET. This device will use the local oxidation of silicon (LOCOS) process for device isolation, which creates a gradual step of approximately 1800 Å between the field oxide and the active area. The Hybrid AFM / STM is designed as a robust SPL system, capable of high-speed patterning and suited for real patterning applications. It may be extended to reliable patterning with multiple probes by incorporating simultaneous and independent feedback for both force and current to each tip.

# VI. Fast Writing With SOG

It is imperative to increase SPL writing speeds if we are to pattern larger areas in reasonable times. We have identified a resist material that is suitable for high speed, nanometer scale lithography using the AFM. The material is siloxene, a Si-O polymer with attached methyl groups, commonly known as Spin-on-Glass (SOG). SOG is a material commonly used in fabricating silicon integrated circuits. It is generally used as a planarizing layer to provide smooth surfaces for photolithography. We have found that SOG can be easily patterned with electrons emanating from a scanning tip.

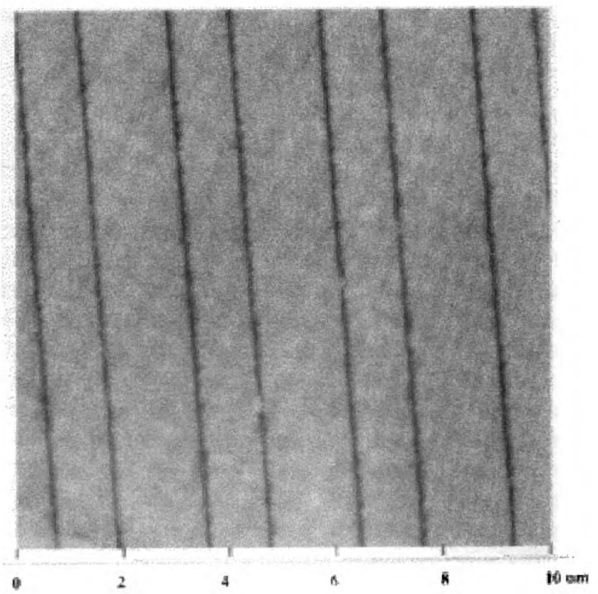
The siloxene type of SOG consists of a methyl (CH3) group and silanol groups (Si-OH) bonded to the Si atoms in the Si-O backbone. The organic content refers to the amount of methyl group, which is proportional to number of Si-C bonds. SOG films with high organic content have superior mechanical properties: lower deposition stress, higher resistance to cracking, and lower film shrinkage. These all contribute to its planarizing properties. The silanol group (Si-OH) with its high polarization (Si-O-H+) is a site for absorption of water. Thus SOG readily absorbs water molecules.

We speculate that when SOG films are exposed with electrons the methyl group is decomposed, thereby decreasing the organic content. We believe that the generated dangling silicon bonds are filled with the silanol group. The wet etch rate of an SOG film in buffered oxide etch (BOE) decreases exponentially with increasing organic content. Thus we can achieve a large etch selectively between exposed and unexposed regions, making SOG an effective resist material for SPL.

In this experiment, we used methylsiloxene SOG (ACCUGLASS-111, Allied Signal Inc.) with 11 percent organic content. The sample substrate was a 2.5 Ω-cm n-type Si (100) wafer. The SOG was spun onto the wafer at 5 krpm for 20 seconds. The wafer was then ramped to 280°C for 5 minutes. We mounted the sample in the AFM (Autoprobe CP, Park Scientific Instruments) operating in contact mode in air. The sample was attached to the sample holder with conducting colloidal graphite and the sample holder was insulated from the piezo scanner. We used a silicon cantilever with a force constant of 2.8 N/m and a 10 nm nominal tip radius of curvature. A positive voltage of 70-100 V was applied to the sample. The electric field near the tip is intense and induces the field emission of electrons from the tip. We measured the current using a current-to-voltage converting amplifier. The measured current ranged from 0.5 to 3.0 nA.

After the current has settled to the desired value, lines were written over the sample across a 90 × 90 μm area at a predetermined scan speed. The scan speed was varied from 180 μm/s to 3024 μm/s. Larger scan areas and higher scan speeds were limited by the response of the piezo scanner. After exposure, the sample was etched in 100:1 BOE for 15 seconds, rinsed in deionized water for 2 minutes, blown dry with nitrogen, and transferred back to the AFM for imaging. No latent image appeared if the sample was scanned with the AFM immediately after exposure and before develop-

**Figure 15**
*AFM micrograph of siloxene SOG patterned with constant voltage AFM lithography. The 100-nm features were patterned at a tip velocity of 1 mm/s.*



ment. This verifies that there is no change in topography during exposure.

The unexposed region etched at a rate of 3.6 Å/sec and the etch selectivity was 20:1 between the exposed and unexposed regions. Figure 15 shows features written in SOG at a scan speed of 1 mm/sec and a current of 2.0 nA at 78 V. The depressions (darker contrast) correspond to the regions of the SOG scanned by the tip. The linewidth obtained from an analysis of the AFM image shows the resolution to be near 100 nm. The corners of the lines do not exhibit any proximity effect, which is a problem with direct write e-beam lithography. We have written patterns with linewidths of 100 nm in SOG with scan speeds as high as 3 mm/sec.

In summary, we have demonstrated nanometer-scale AFM lithography of siloxene SOG films at high scan speeds. Writing speeds as high as 3 mm/sec were performed. We believe that SOG can be patterned at higher speeds as long as the correct dose of electrons is delivered. In practice, the speed of lithography is limited by the response of the scanner. Minimum resolution of 40 nm has been demonstrated. The patterns show no proximity effects. The width of the lines are controlled by the dose, smaller doses producing finer features. The etch selectivity may be increased by controlling the organic content, which is governed by the electron dose. The study of pattern profile and the exact nature of material modification remains a topic for future investigations.

# VII. Summary

The most important limitation on the scanning probe microscope for imaging or lithography is its low throughput. We believe that the best way to increase throughput is to image or pattern with arrays of parallel cantilevers. In this paper we have described recent work toward high speed patterning. By integrating ZnO piezoelectric actuators onto each cantilever, we have imaged in constant force mode where the setpoint force is maintained by each of the two cantilevers. The resonance of the ZnO cantilevers when in contact with the sample surface is near 44 kHz, which allows high speed scanning. We have also described two different deflection sensors, the piezoresistive cantilever and the interdigital cantilever, which are suitable for parallel array operation. Finally, we discuss our work on scanning probe lithography. Amorphous silicon is an attractive resist since it can be deposited on virtually any surface and can be patterned in both the positive and negative tone. Organic polymer resists show promise for high speed writing and reduced tip wear. Most notably, we have patterned 100-nm features in SOG at speeds as high as 3 mm/s. We have also designed the Hybrid AFM / STM lithography system, which combines the key features of the AFM and STM by incorporating two independent feedback loops to control both force and current. This system is capable of patterning organic resists spun over topography and may be extended to reliable patterning with multiple probes. We believe that increased throughput will make scanning probes a viable alternative for critical dimension lithography in the semiconductor industry and for high density storage applications.

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# Biographies

Kathryn Wilder received the B.S. degree from Yale University in 1994 and the M.S. degree from Stanford University in 1996, both in applied physics. She is currently working toward the Ph.D. degree in applied physics at Stanford. Her thesis research is on scanning probe lithography.

Hyongsok T. Soh received a B.S. degree with Distinction in 1992 with a double major in Mechanical Engineering and Materials Science, and an M.Eng degree in 1993 in Electrical Engineering all from Cornell University. He is currently working on the Ph.D degree in Electrical Engineering at Stanford. His research is on scanning probe lithography and nanometer scale electron devices.

Stephen C. Minne received a B.S. with highest honors from the University of Illinois U-C in 1992, and a M.S. and a Ph.D. from Stanford University in 1994 and 1996 respectively. His thesis work was on increasing the throughput of the AFM. He currently holds a position as a Research Associate at Stanford University.

Scott R. Manalis received the B.S. in physics with highest honors from UC Santa Barbara in 1994, and the M.S. from Stanford University in 1995. He is currently working on the Ph.D. degree in applied physics at Stanford in the area of scanning probe microscopy and lithography.

Calvin F. Quate, Ph.D., is the Leland T. Edwards Professor of Electrical Engineering (Research) at Stanford University. Awards include the Rank Prize for Opto-Electronics (1982), IEEE Medal of Honor (1988), and the President's National Medal of Science (1992).

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# Research Notes

## Positioning System for Nanolithography

The lithographic techniques described in the various articles in this special issue have been developed to fabricate circuit features which can be of the order of 10 nm in size. To fabricate an entire circuit, one must be able to position these features at precisely defined locations on a wafer surface and one must be able to return to a specific location with precision for subsequent processing levels. Thus, pattern placement and repeatability are critical issues. In order to address this need, an ONR Small Business Innovative Research (SBIR) project was awarded to OPTRA, Inc. of Topsfield, Massachusetts to develop a positioning system capable of a precision of 5 nm or better over an entire 4-inch wafer. It was specified that an STM must be integrated into this positioning system and that the system must operate in a high vacuum environment. The plan is to delivery this system to NRL in September 1997 for use in their nanolithography program.

A generic positioning system consists of an actuator, a position sensor, and a feedback loop which minimizes error between programmed and actual positions. The most sophisticated positioning systems presently in use in the semiconductor industry employ a laser interferometer as a position sensor. The laser is a conventional He-Ne laser and the optical path is typically a few meters in length. These laser interferometers are expensive and are subject to errors due to atmospheric fluctuations. Measurements have shown that fluctuations due to ordinary room noise can cause position errors of the order of 10 nm. Errors of this magnitude are unacceptable in the world of nanoelectronics.

The OPTRA approach is based on diffraction of light from a grating. The light source is an inexpensive laser diode, and position is determined by measuring the diffraction pattern with an array of three photodiode detectors. The position sensor consists of a diffraction grating measuring 4 inches on a side and a sensor head (containing the laser, the optics and the detectors) the size of a computer mouse. Since the optical path is very short, the sensor is not susceptible to atmospheric fluctuations. Furthermore, the cost is expected to be a fraction of that of present commercial laser interferometers. The required system performance has been demonstrated at OPTRA in laboratory measurements, and work is proceeding on the final system for delivery.